



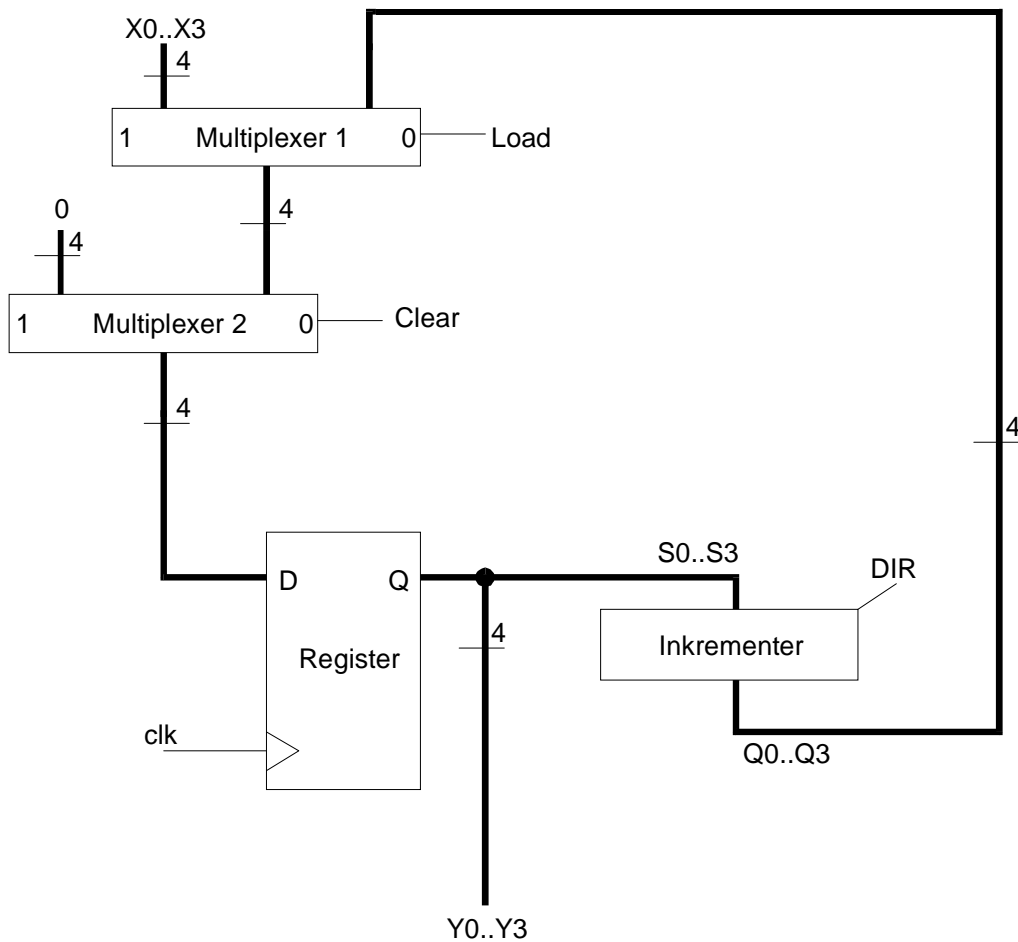
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Lab 3  
Designing combinatorial and sequential circuits

Exercise 1

The first part of this exercise is to integrate the counter designed in Exercise 2 of Lab 2 into the circuit shown below. To make the 4-bit counter in Illustration 1 you will need to create two separate units: 4-bit multiplexer; and then a 4-bit register. Once the design is complete, compile and simulate it.



*Illustration 1: 4-Bit Counter*

## Exercise 2

The 4-Bit counter from the previous exercise can be used to make a “running light” out of the eight LED lights on the board. A running light is when you have only one of the eight LED lights on, and then when a clock is applied, the “on” LED moves LEFT or RIGHT by one LED. This is similar to Exercise 1 from the first Microprocessor Programming Lab. To do this you will need to create a 3-bit decoder that uses the outputs  $Y[3..0]$  from the counter to decide which of the 8 LED lights to turn on. For example, when the input to the decoder is “5”, then LED number “5” is on.

Complete this exercise using a GDF file. Compiling and simulation should be done with the EPM7128SLC84-15 FPGA selected.

When your group is finished with the lab you must submit all GDF, SYM, VHD and SCF files. Please make sure the names of these files are appropriate (eg. myFullAdder.GDF). Also, please compress your final submission into one ZIP file before submitting it using the web page portal.