ALBERT-LUDWIGS-
UNIVERSITÄT FREIBURG

INSTITUT FÜR INFORMATIK

Prof. Dr. Bernd Becker
Dipl. Inf. Tobias Schubert
M. Sc. (Eng.) Matthew Lewis

Mobiles Hardware-Praktikum
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Lab 2
Designing combinatorial and sequential circuits

Exercise 1

Implement and simulate the arithmetic and logic unit (ALU) from exercise 2 of the previous Lab using VHDL. It may be help to use a State Diagram to figure out the key signals. To simplify the design you don't need to include input and output pads. Lastly, add a multiply (A*B) unit and its control signals to the ALU.

Exercise 2

Create a graphical GDF file for a 4-bit incrementer circuit with inputs S[3..0] and DIR, and outputs Q[3..0]. The DIR input is the control input. When DIR=0 then Q[3..0] = S[3..0] + 1, and when DIR=1 then Q[3..0] = S[3..0] - 1. Simulate your design and produce a symbol for the incrementer. Again use the EPM7128SLC84-15 FPGA.

When your group is finished with the lab you must submit all GDF, SYM, VHD and SCF files. Please make sure the names of these files are appropriate (eg. myFullAdder.GDF). Also, please compress your final submission into one ZIP file before submitting it using the web page portal.