ALBERT-LUDWIGS-UNIVERSITÄT FREIBURG

INSTITUT FÜR INFORMATIK

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Lab 1
Designing combinatorial and sequential circuits

Exercise 1

This first exercise is to create a simple arithmetic unit that can be controlled to add and subtract two 4-bit numbers (a 4-Bit adder/subtracter). The procedure is as follows:

- First, startup the MAX+PLUS II BASE LINE software and open a new „Graphic Design File“ (GDF). Design a half-adder and then compile it for the EPM7128SLC84-15 Altera FPGA. Then create a symbol for this component so that it can be used in the following steps.

- Now, open a new GDF file and create a full adder using the half adder you designed in the previous step. Compile your circuit and then simulate it to insure proper functionality.

- Use the full adder to develop a 4-Bit Conditional Sum adder. Define the inputs and the outputs of the circuit as buses to simply the circuit and to make it more legible (refer to *MAX+PLUS II Getting Started*, pg. 181ff). Then find the delay of the circuit by running a timing Simulation. Remember that the total delay is from the time the input is applied until the highest order bit in the result is calculated.

- Lastly, using the 4-bit adder implement above build a 4-bit adder/subtracter circuit as described in the *Technische Informatik II* lectures. Compile this final design and simulate to insure correctness.

Exercise 2

The idea of this exercise is to use the adder/subtracter circuit you created in exercise 1 to construct a 4-bit arithmetic and logic unit (ALU) with the functionality shown in illustration and table 1. So, depending on the opsel[1..0] and Clear control signals, the ALU should either output the addition(A+B) or subtraction(A-B) of the two 4 bit inputs, or output all zeros in the case that the Clear bit is high. To simplify matters, don’t worry about performing addition or subtraction on numbers who’s results are out of the range of this 4-bit ALU.

Another requirement of the circuit is for you to add a register or latch for the opsel[1..0] and Clear signals. This insures that the function performed by the ALU only changes when a clock or push button event occurs.

+	-	Clear	opsel1	Opsel0	Funktion
0	0	0	X	X	---
0	0	1	0	0	Output set to 0
1	0	0	0	1	Addition
0	1	0	1	0	Subtraction

Table 1: Arithmetic and logic unit functionality

Implement your arithmetic unit as a GDF file with the MAX+PLUS II software and then compile and simulate it for the EPM7128SLC84-15 FPGA.

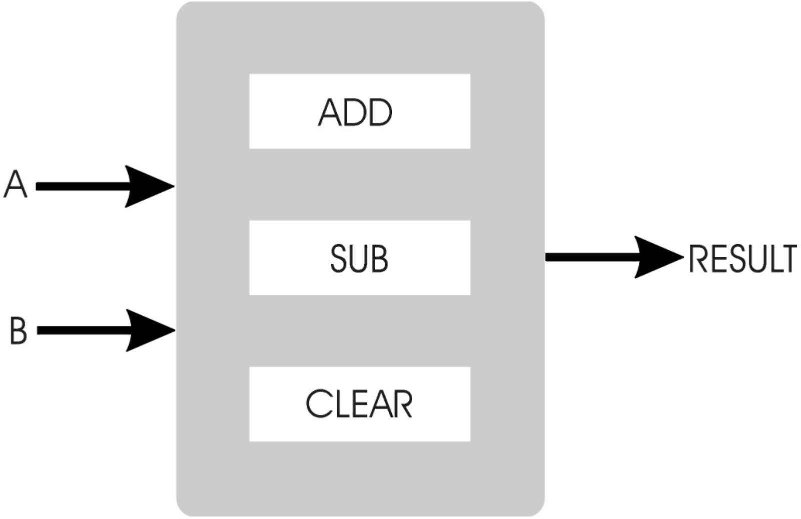

Illustration 1: The planned arithmetic and logic unit

When your group is finished with the lab you must submit all GDF, SYM, VHD and SCF files. Please make sure the names of these files are appropriate (eg. myFullAdder.GDF). Also, please compress your final submission into one ZIP file before submitting it using the web page portal.