

The PICee Development System's Extension Modules

In order to complete all the labs in this course, you will need to have a good understanding of the PICee development system (Illustration 1) and the two extension boards that come with it. The first extension board is the experimentation board. It has many open sockets, pushbuttons, and switches and is shown in illustrations 2. The second extension board is the FPGA board and it is shown in illustrations 4. Both extension boards have a 64-pin contact strip that can be connected to the contact strip on the main PICee board. The connecting strip acts like a large data bus to enabling bi-directional communication between the extension boards and the main PICee board. The shared signals are (these are also labeled on the boards):

- PORTA0..4
- PORTB0..7
- VCC
- GND
- Reset
- Clock signals OSC1/2

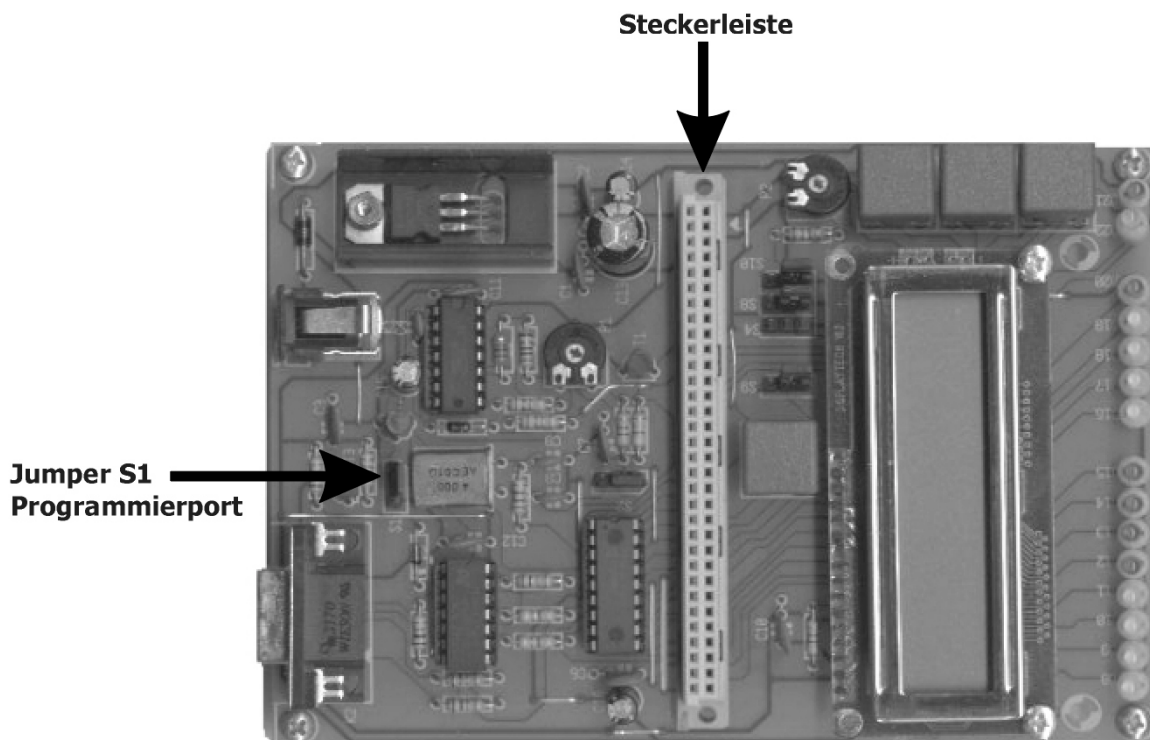


Illustration 1: The PICee development system

The PIC16F84 microprocessor has two operating modes (program and run mode) that are controlled by jumper S1. When either one of the extension boards is mounted on the main PICee board the jumper cannot be accessed. To overcome this, a switch and connecting cable is provided on both extension boards. This switch allows you to switch between the program and run mode (P=program mode, R=run mode).

The experimentation board (illustration 2 and 3) is a freely configurable board and can be used to build and analyze a range of complex circuits. It has room for both analog and digital components while also providing many free connection points so that wires can be easily

added. The PIC16F84 microprocessor can also interact with this board, controlling or monitoring custom built circuits.

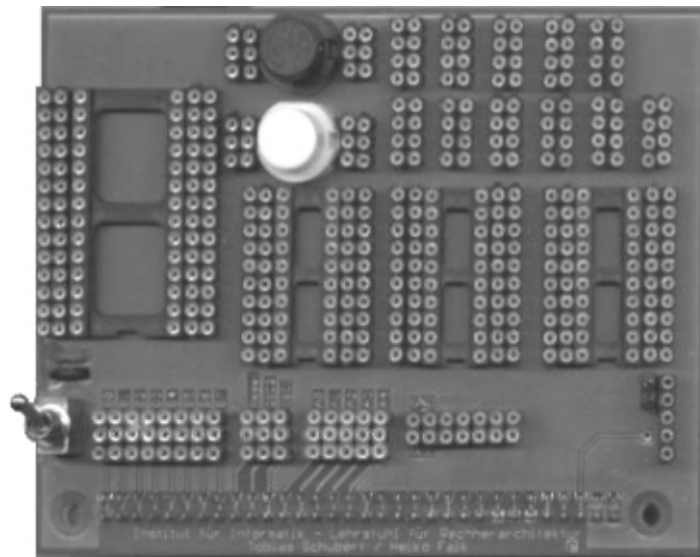


Illustration 2: The experimentation extension module

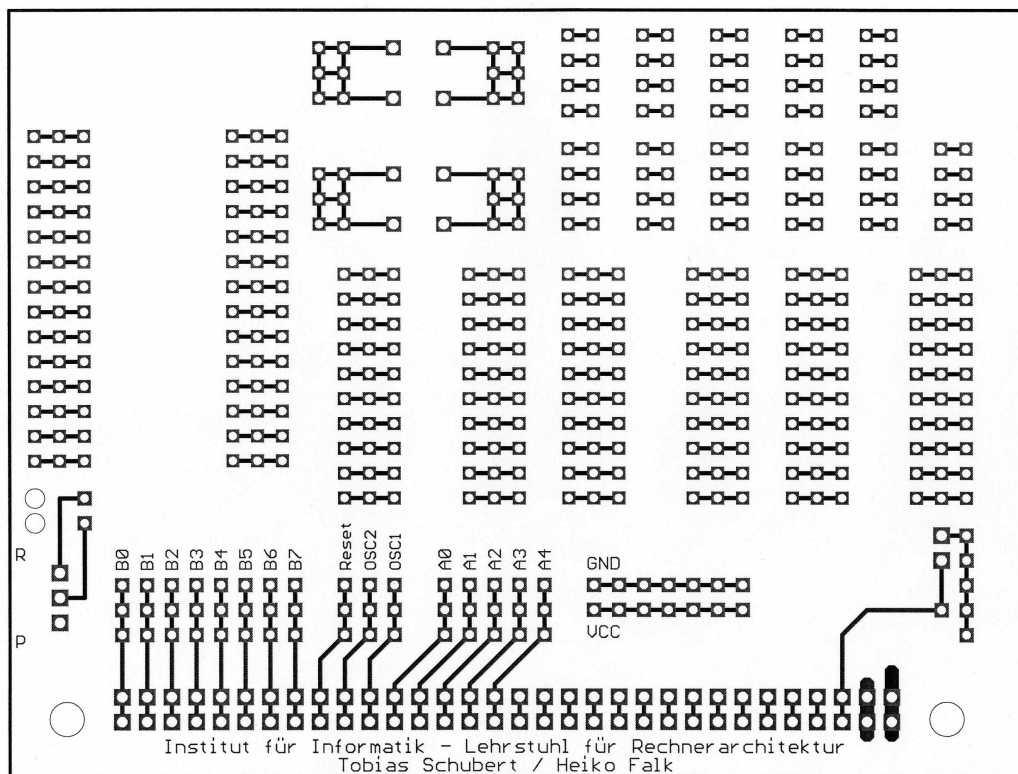


Illustration 3: The experimentation extension module board schematic

The FPGA extension board (illustration 4, 5, and 6) contains an EPM7128SLC84-15 FPGA from Altera. This FPGA can be programmed with the use of the *MAX+PLUS II Baseline* software and a free parallel port. Some things to consider when using this board are:

- All of the FPGAs pins are directly accessible using the two rows of sockets that surround the FPGA.
- The allocation of the pins to their appropriate sockets is shown in illustration 7.
- VCC and GND are already connected to the FPGA.
- The global clock (pin 83) is already connected to the FPGA. The global clock comes from OSC1 and is the same clock that is used by the main PICee board.

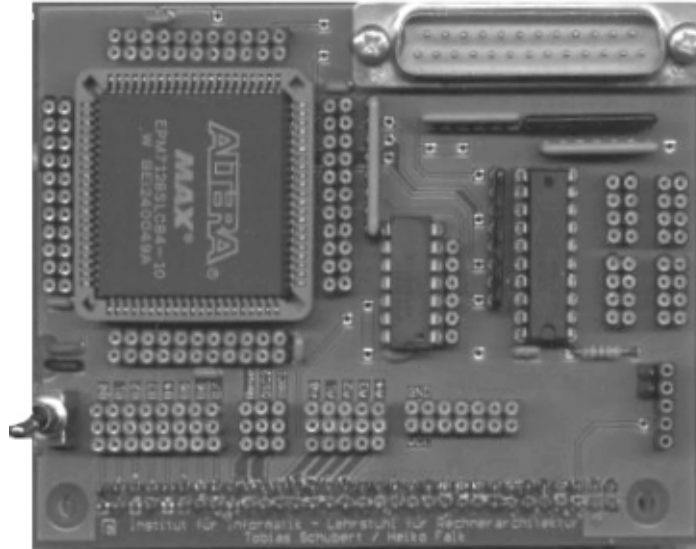


Illustration 4: The FPGA extension module

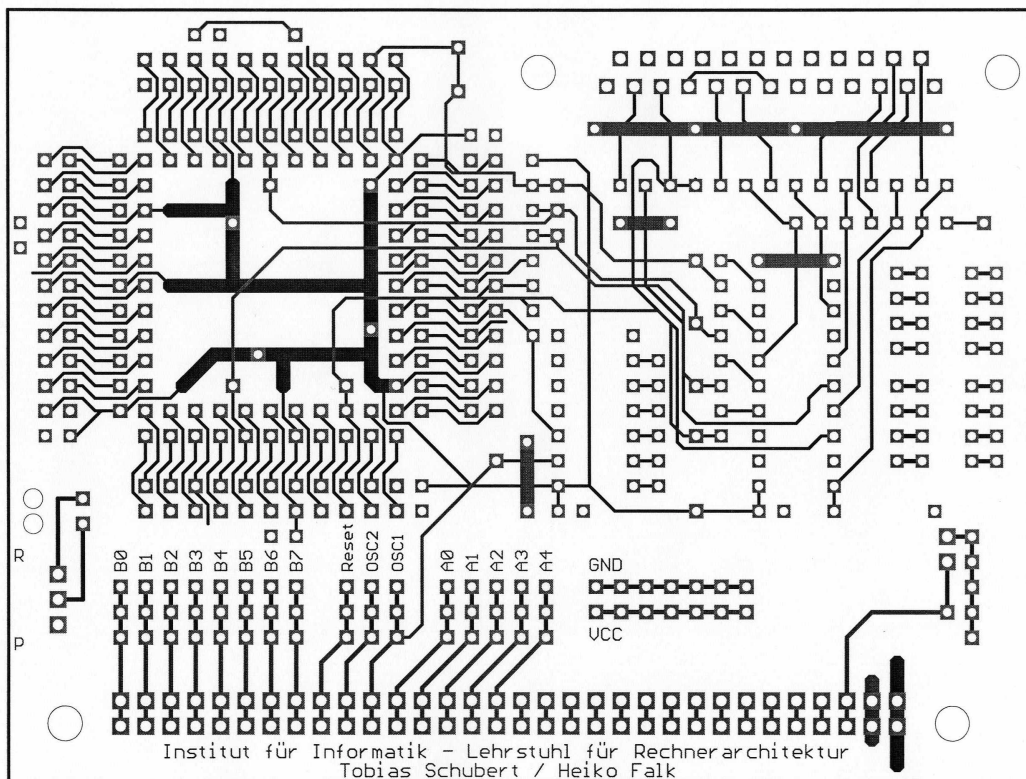


Illustration 5: The FPGA extension module schematic

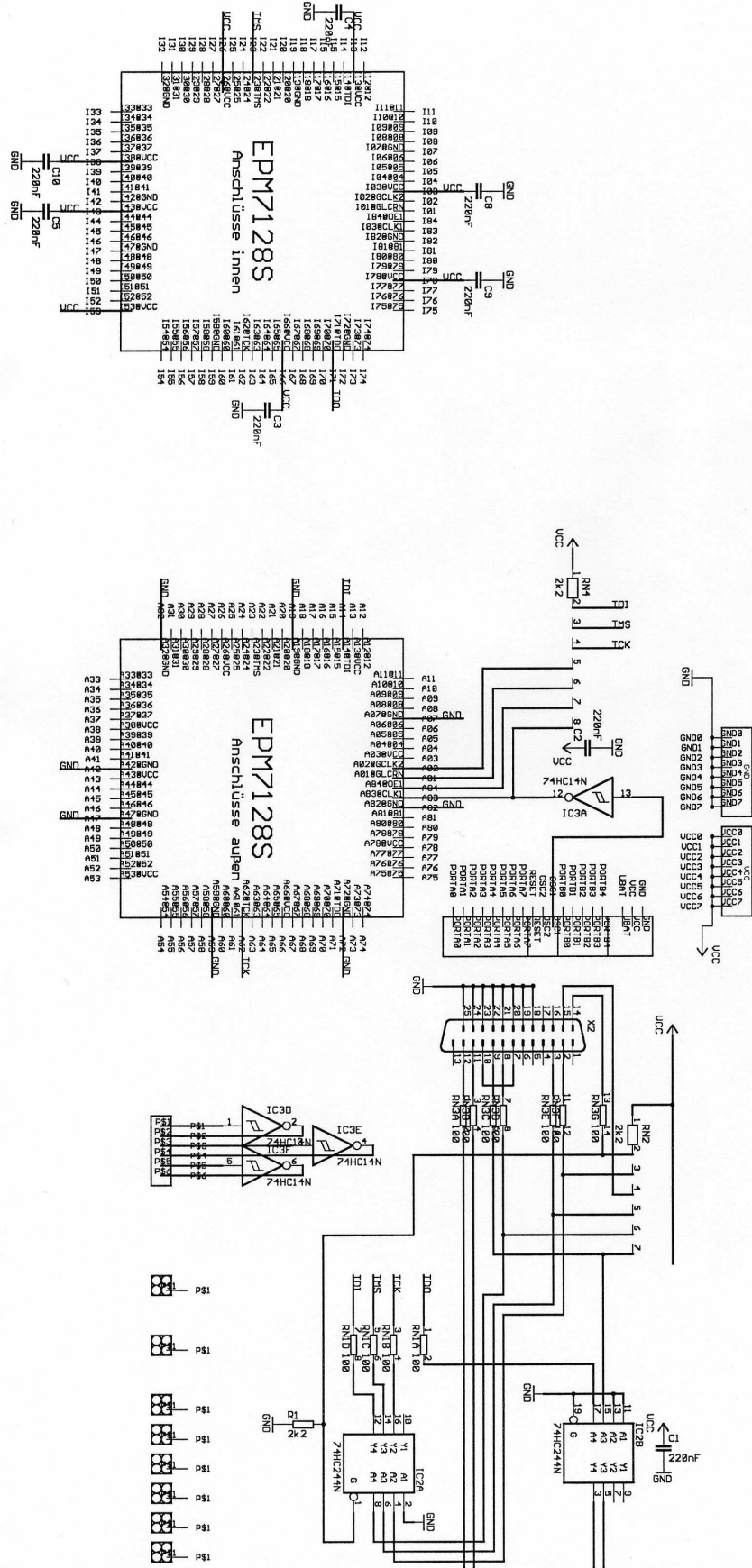


Illustration 6: FPGA extension module connection diagram

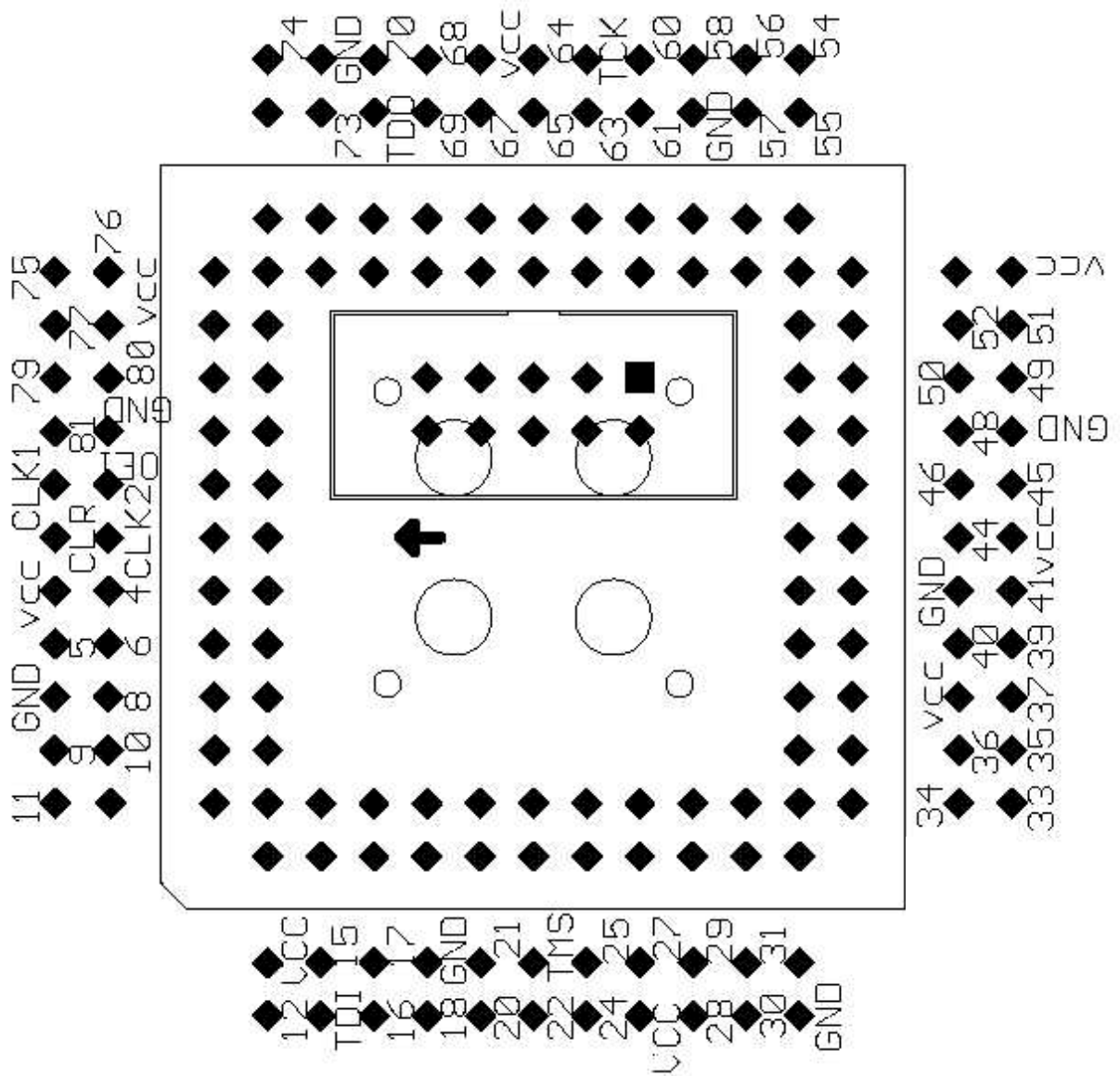


Illustration 7: FPGA EPM7128SLC84-15 pin allocation