Delta-IDDQ Testing of Resistive Short Defects*

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Abstract

This paper addresses the efficiency of IDDQ and more specifically Delta-IDDQ testing when using a realistic short defect model that properly considers the relation between the resistance of the short and its detectability. The results clearly show that the Delta-IDDQ approach covers a large number of resistive shorts missed by conventional logic testing, requiring only a relatively small vector set. In addition a significant number of defects which are proven to be undetectable by logic testing but may deteriorate and result in reliability failures are detected. The Delta-IDDQ threshold and thus the equipment sensitivity is shown to be critical for the test quality. Furthermore, the validity of the traditional IDDQ fault models when considering resistive short defects is found to be limited. For instance, the use of the fault-free next-state function for sequential IDDQ fault simulation is shown to result in a wrong classification of some resistive short defects. This is the first systematic study of IDDQ testing of resistive short defects. The impact of the threshold on the defect coverage is quantified for the first time. Although the simulation results are based upon a 0.35µm technology, the results and methodology can be transferred to state-of-the-art and NanoTechnologies.

Keywords: IDDQ testing, Delta-IDDQ, Resistive defects, Early-life failures

1 Introduction

Quiescent current (IDDQ) testing has been argued to be ineffective for state-of-the-art CMOS circuits due to relatively high and variable leakage currents even in defect-free ICs. This is only partially correct [1]. It is true that the classical assumption that a defect-free CMOS circuit does not conduct any current when it is not switching (IDDQ = 0) does not hold anymore. There is a non-negligible *background IDDQ current* I_{back} flowing through the circuit irrespective of whether it is defective or not. It is composed of leakage currents I_{off} of the OFF transistors. Although the contribution of every individual transistor is negligible, the cumulative effect of millions of the transistors is significant. Low-V_T transistors used in high-performance logic are particularly prominent contributors to I_{back}.

This problem is addressed by design measures as well as by a number of advanced test methodologies like relative IDDQ, current ratios, current signatures, and Delta-IDDQ [2, 3]. In this work we will consider Delta-IDDQ testing. It is based on detecting the *difference* in the amount of current flowing through a defective circuit depending on whether the defect is activated or not. Delta-IDDQ testing is supported by measurements at different vector locations.

Assume a short defect between nodes a and b. Suppose that the test set includes two test vectors t_1 and t_2. t_1 sets the nodes a and b to the same logical value (e.g., $a = b = 0$), while t_2 sets a and b to opposite values (e.g., $a = 1$, $b = 0$). Under t_1, the background current IDDQ$= I_{back}$ is measured. Under t_2, there is a conducting path from V_{DD} through the PMOS network driving the node a, the short defect and the NMOS network driving the node b to ground. As a consequence, some current I_{defect} will flow through this conductive path and the total measured current will be IDDQ$= I_{back} + I_{defect}$. If no such elevated current is measured for t_2, then it is assumed that there is no short defect between a and b.

There are essentially two criteria for the applicability of Delta-IDDQ testing to today's advanced technologies. The first relates to the current measurement equipment that must be sufficiently fast (to satisfy test time and cost constraints), *and* sensitive to enable distinguishing between I_{back} and $I_{back} + I_{defect}$, as to be able to identify small variations on top of large background currents. Secondly in function of defect detection itself, the vector set used should contain at least one vector that activates the defect and *at least one vector that does not activate the defect*, as defects that are being activated by all vectors are escaping a Delta-IDDQ approach. Preferably, but not a must, the variation of I_{back} is small compared with I_{defect}, as this affects the screening efficiency. This might *not* be the case for some large high-performance parts such as the largest microprocessors on the market. For many other products, however, including low-power designs with high-V_T transistors with well-controlled leakage, Delta-IDDQ testing is applicable by selecting a value ΔI_{limit} and identifying the parts for which the measured current under different test vectors differs by at least ΔI_{limit} Ampere. Note that this procedure is still effective if I_{back} is not constant for different circuits, as the actual decision is die rather than product related. In general, the variation of I_{back} of the same die (in absence of defects) for different vectors tends to *decrease* for larger ICs, because this variation occurs if a very large fraction of transistors are active under one input vector and very few transistors are active under a different test vector. As the total number of transistors becomes large, the probability that very large fraction of them are active (or not) simultaneously is reduced. This is clearly beneficial for Delta-IDDQ testing.

This paper studies the detection of resistive shorts by IDDQ and more in particular Delta-IDDQ testing. In contrast to [4, 5], we do not consider resistive intra-gate shorts

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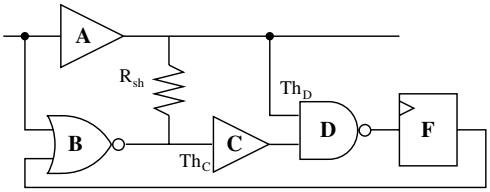

Figure 1: Example circuit

or shorts between two inputs of the same gate, as our assumptions on the I-V characteristics do not hold for such shorts. Similar to the approach initially developed for conventional (voltage) testing [6, 7, 8], we derive a *detectability interval* for a given short defect (the interval contains all the defect resistance values for which the defect is detected by IDDQ measurements) and several parametric *fault coverage metrics*. The metrics accurately distinguish between the defects which can change the logical function of the circuits and defects that are proven to be redundant from the logical point of view at time zero, but either heal or deteriorate over time causing early-life failures and field returns.

It turns out that some of the assumptions traditionally made for IDDQ testing do not hold unconditionally when resistive shorts are under consideration. One instance is the fault simulation of sequential circuits. It was claimed in [9] that it is safe to use the fault-free next-state function for calculating fault coverage. It has been noted in [10] that this does not hold for certain resistive shorts which modify the values stored in the flip-flops. We demonstrate that our technique will yield the correct detection conditions even for such non-trivial cases. Moreover, the correct detection interval will be non-contiguous. This is unexpected because the only source of such intervals are reconvergencies of paths starting at the defect site and the conventional wisdom states that fault effect propagation is irrelevant in IDDQ testing.

The experimental results show that Delta-IDDQ testing is effective in detecting defects not covered by conventional logic testing including both detectable and logic undetectable defects. This holds even if a reduced number of test vectors is employed. However reducing the number of vectors reduces the chances that the Delta-IDDQ criteria are met, with reduced fault coverage as result. We also observe a relation between the threshold current ΔI_{limit} and the test quality. In function of high quality test requirements (like Automotive and Medical) the use of a small delta limit is advantageous as it helps to identify subtle defects before they affect the operation of the circuit.

The remainder of this paper is organized as follows. The fault model for resistive shorts with respect to Delta-IDDQ testing is described in the next section. The anomalous behavior of a resistive short is demonstrated in Section 3. Experimental results are reported in Section 4. Section 5 concludes the paper.

2 Resistive Short Detection by IDDQ

This section will introduce the resistive short fault model used for the analysis in this paper. Fault effects on both the voltage and the current are modeled and a non-trivial interaction of these effects is demonstrated later on. Consequently, some basic definitions and concepts for the conventional (non-IDDQ) case in which the detection is based on the logic value (voltage) are essential for understanding the model. Although they have been published elsewhere [11], we recapitulate them briefly in order to make the

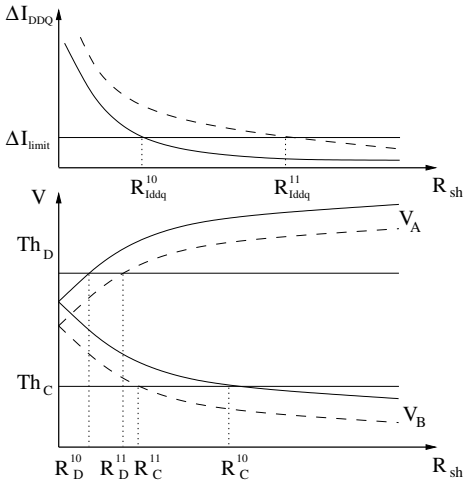

Figure 2: Voltage and current characteristics

paper self-contained. We use an example circuit for illustration. The same circuit will be used later on to demonstrate the anomalous behavior in the sequential case. Note that only voltage effects have been considered in previous works and all the material regarding the current effects is new.

2.1 Analogue Detectability Intervals for voltage and current

A resistive short defect between two lines driven to opposite logic values will result in intermediate voltage levels on these lines. The exact value of the voltage is determined by the electrical parameters of the gates which drive the shorted lines, the logical values applied to the inputs of these gates (which determine the number of ON transistors in the gates), and the value of the short resistance R_{sh}. This voltage will be interpreted as either logic 0 or logic 1 by the succeeding gates, i.e., gates fed by the shorted lines, depending on the *logic threshold* Th of these gates. The interval of all R_{sh} values for which the faulty logical value is interpreted on a line is called *Analogue Detectability Interval* or ADI.

Figure 1 shows an example sequential circuit which consists of two buffers A and C, one NOR gate B, one NAND gate D and one flip-flop F. The outputs of gates A and B are shorted by a defect of unknown resistance. Assume that F stores the logical value of 0 and that logic-1 is applied to the input of the circuit. The voltage potentials V_A and V_B on the lines driven by gate A and gate B, respectively, as function of the short defect resistance R_{sh}, are shown in the lower part of Figure 2 as solid lines. The logic threshold of gate C is Th_C, and the logic threshold of the upper input of gate D is Th_D. The thresholds are independent of R_{sh}; they are shown as horizontal lines. The R_{sh} value for which a voltage characteristic crosses a threshold is called *critical resistance*. The critical resistance is used for determining the ADI. For example, R_D^{10} for gate D, i.e., gate D interprets the voltage on the line driven by A as logic-0 if $R_{sh} < R_D^{10}$ and logic-1 otherwise (the superscript '10' refers to the values seen by gate B). Since the fault-free value is logic-1, the ADI on the upper input of gate D is $[0, R_D^{10}]$. The ADI on the input of gate C is $[0, R_C^{10}]$. This ADI propagates through gate C to the lower input of gate D. It is easily checked that the faulty logical value (0) is assumed at the output of gate D if $R_D^{10} < R_{sh} < R_C^{10}$, i.e., the ADI is $[R_D^{10}, R_C^{10}]$.

The solid curve in the upper part of Figure 2 shows the current flowing through the defect site as a function of R_{sh} if the flip-flop stores a logic-0 and a logic-1 is applied to the input of the circuit. The Delta-IDDQ threshold ΔI_{limit} is shown as a horizontal line. There is also a critical resistance R^{10}_{Iddq}: for all R_{sh} values below R^{10}_{Iddq} the defect-induced current will surpass the Delta-IDDQ threshold and will be detected. We refer to the R_{sh} interval in which the extra current exceeds ΔI_{limit} as I-ADI (in the example, I-ADI = $[0, R^{10}_{Iddq}]$).

If the value in the flip-flop is logic-1 instead of logic-0, two NMOS transistors (instead of one) are ON in gate B. As a consequence, the voltages on both shorted lines decrease and the current increases for a given R_{sh} value. This is shown in Figure 2 by dashed lines. Note that the values of the critical resistances change (indicated by superscript '11').

The ADIs for logic (voltage-based) detection are aggregated for all test vectors of a given test set to form C-ADI (covered ADI). The R_{sh} range for which the defect can be detected by at least one test vector is called G-ADI. Thus, a defect with $R_{sh} \in C$-ADI has been detected by a given test set; a defect with $R_{sh} \notin G$-ADI is undetectable by voltage testing. C-ADI is always included in G-ADI. In contrast, Delta-IDDQ testing detects short defects with R_{sh} values in some interval I-ADI which may or may not be part of G-ADI.

2.2 Electrical model

Similarly, from a current perspective a resistive short defect between two lines driven to opposite logic values will result in a current flowing through the defect, which is function of the short resistance R_{sh}, and in intermediate voltage levels on these lines, also function of R_{sh}. The latter will cause additional current to flow through the gates driven by the lines affected by the defect. In the remainder of the paper we will take a conservative position and only consider the current flowing through the defect itself and not the secondary current increase. As such we will consider a pessimistic boundary on the fault coverage figures.

The critical resistance for Delta-IDDQ testing is the highest value of the short resistance R_{sh} for which the current flowing from V_{DD} to ground through the defect exceeds the Delta-IDDQ threshold ΔI_{limit}. It is determined using a procedure similar to the one employed to calculate the critical resistance for logic testing, i.e., to determine the highest R_{sh} which makes a succeeding gate interpret a faulty logical value.

Let $n1$ and $n0$ denote the shorted lines driven to opposite logic values. Let $n1$ ($n0$) be the line driven to logic-1 (logic-0) by the PMOS (NMOS) network. The following system of equations holds [12, 7, 13]:

$$\left\{ \begin{array}{rcl} I_0 & = & I_p(V_{DD} - V_{n1}) \\ I_0 & = & I_n(V_{n0}) \\ R_{sh} & = & (V_{n1} - V_{n0})/I_0 \end{array} \right. \quad (1)$$

where V_{n1} is the voltage potential on $n1$, V_{n0} is the voltage potential on $n0$, $I_p(V)$ is the I-V characteristic of the PMOS network, $I_n(V)$ is the I-V characteristic of the NMOS network and R_{sh} is the short defect resistance. Essentially, the current flowing through $n1$, short defect and $n0$ must be equal because no current sink or source exists on the path. The value of the current is called I_0. I_0 is the defect-induced contribution to the overall quiescent current flowing through the circuit. The background current

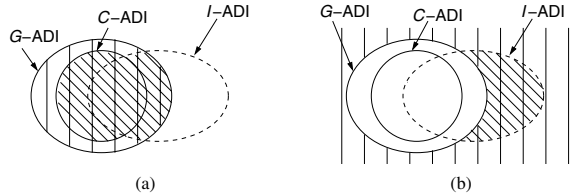

Figure 3: Venn diagram for (a) combined fault coverage FC^{Iddq}_{comb} (Eq. (5)), (b) flaw coverage FC^{Iddq}_{flaw} (Eq. (6)). Diagonal lines indicate the nominator, vertical lines show the denominator.

I_{back} is assumed to be independent of the defect; consequently, it is regarded as a constant offset which does not influence defect detection. The analysis is hence valid for Delta-IDDQ.

To calculate the critical resistance R^{logic}_{crit} for the case of logic testing, one of the voltages (e.g., V_{n1}) is set to the logic threshold Th of the succeeding gate in question and the equation system is solved to obtain three values V_{n0}, I_0 and R_{sh} from three equations. The critical resistance is determined from $R^{logic}_{crit} = R_{sh}$. I-V characteristics I_p and I_n are given by the technology in which the driving gates are implemented and the number of ON transistors in these gates (see [13] for details and three examples of technology-specific models).

In case of Delta-IDDQ, we use the same three equations to quantify the extra contribution of the defect to the IDDQ of the affected cells, compared with the current in the defect free case. We set $I_0 = \Delta I_{limit}$ and determine V_{n1}, V_{n0} and R_{sh} from the equations. The critical resistance for Delta-IDDQ testing is given by $R^{Iddq}_{crit} = R_{sh}$. The equation for the case of a two-inverter short assuming the validity of Shockley equations is:

$$R^{Iddq}_{crit} = \frac{1}{\Delta I_{limit}} \left(|Vt_p| + \sqrt{(V_{DD} - |Vt_p|)^2 - \frac{2 \cdot \Delta I_{limit}}{\beta_p \mu_p C_{ox}}} - V_{DD} + Vt_n + \sqrt{(V_{DD} - Vt_n)^2 - \frac{2 \cdot \Delta I_{limit}}{\beta_n \mu_n C_{ox}}} \right) \quad (2)$$

where β is the width-length ratio, μ is the mobility, V_{DD} is the power supply voltage, Vt is the transistor threshold, C_{ox} is the oxide capacity and ΔI_{limit} is the Delta-IDDQ threshold. Indices p and n indicate PMOS and NMOS parameters, respectively.

Remind that additional current through a succeeding logic gate will result from a weakened voltage potential on its input. As stated before we do not account for this effect, which means that our current estimate is conservative.

2.3 Fault coverage metrics

The *logic fault coverage* FC^{logic} denotes the detection probability of a fault f and is defined as

$$FC^{logic}(f) = 100\% \left(\int_{C\text{-ADI}} \rho(r) dr \right) / \left(\int_{G\text{-ADI}} \rho(r) dr \right), \quad (3)$$

where $\rho(r)$ is the probability density function of the short resistance r obtained from manufacturing data (i.e., $\rho(R_{sh})$ gives the probability that a short has the resistance R_{sh}). See [14, 15] on the procedures for obtaining $\rho(r)$.

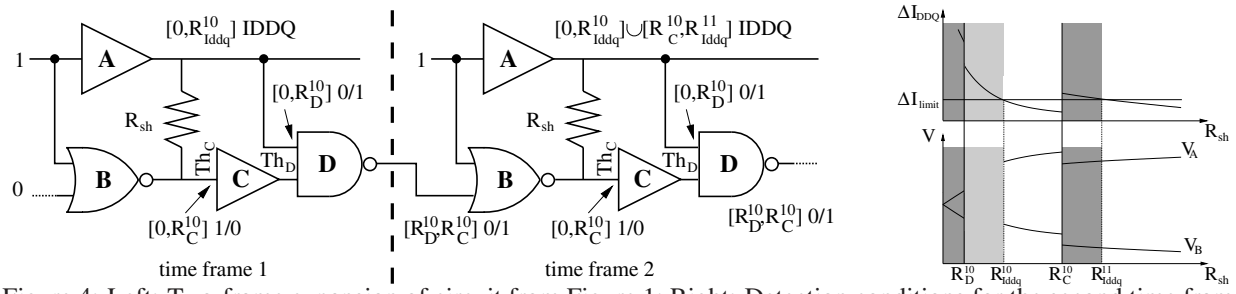

Figure 4: Left: Two-frame expansion of circuit from Figure 1; Right: Detection conditions for the second time frame

The *IDDQ fault coverage* FC^{Iddq} denotes the detection probability of a fault f by IDDQ testing and is defined as

$$FC^{Iddq}(f) = 100\% \cdot \frac{\int_{(I\text{-ADI} \cap G\text{-ADI})} \rho(r)dr}{\int_{G\text{-ADI}} \rho(r)dr}. \quad (4)$$

We define the *combined fault coverage* as

$$FC^{Iddq}_{comb} = 100\% \cdot \frac{\int_{((C\text{-ADI} \cup I\text{-ADI}) \cap G\text{-ADI})} \rho(r)dr}{\int_{G\text{-ADI}} \rho(r)dr}. \quad (5)$$

The next metric definition captures the coverage of *flaws*, i.e., defects undetectable under nominal conditions which may cause early-life failures. $R_{sh} \in [0\Omega, \infty] \setminus G$-ADI holds. The condition for a defect to be detected by Delta-IDDQ testing is $R_{sh} \in ([0\Omega, \infty] \setminus G\text{-ADI}) \cap I\text{-ADI}$. We define the *IDDQ flaw coverage* as the probability that a flaw is detected by Delta-IDDQ testing:

$$FC^{Iddq}_{flaw} = 100\% \cdot \frac{\int_{(([0\Omega,\infty] \setminus G\text{-ADI}) \cap I\text{-ADI})} \rho(r)dr}{\int_{[0\Omega,\infty] \setminus G\text{-ADI}} \rho(r)dr}. \quad (6)$$

All the metrics are defined with respect to one fault; for a fault list average numbers are taken. Figure 3 illustrates the definitions of FC^{Iddq}_{comb} and FC^{Iddq}_{flaw} in form of Venn diagrams.

3 Sequential Behavior

Consider again the circuit from Figure 1. Suppose that two test vectors '1' are applied to the primary input in consecutive clock cycles (i.e., logic-1 is on the input of the circuit in time frames 1 and 2) and that the flip-flop F is reset to logic-0 in the beginning. Recall that in this case the voltage and current characteristics are shown by solid lines in Figure 2 and the critical resistances for logic detection are R^{10}_C and R^{10}_D and the Delta-IDDQ critical resistance is R^{10}_{Iddq}. If logic-1 is in the flip-flop, the characteristics are shown by dashed lines and the critical resistances are R^{11}_C, R^{11}_D, and R^{11}_{Iddq}. We assume $0 < R^{10}_D < R^{10}_{Iddq} < R^{10}_C < R^{11}_{Iddq}$.

Figure 4 (left) shows the two-frame expansion of the circuit. In the first time frame, Delta-IDDQ testing detects the defect in interval $[0, R^{10}_{Iddq}]$ (as discussed above). The value stored in the flip-flop is logic-0 if $R_{sh} \in [R^{10}_D, R^{10}_C]$ and logic-1 otherwise. As a consequence, the characteristics valid for the second time frame correspond to the solid lines from Figure 2 in the interval $[R^{10}_D, R^{10}_C]$ and to the dashed lines elsewhere, as shown in Figure 4 (right). The regions in which Delta-IDDQ testing detects the fault are shown grey or light grey (light grey indicates logic-0 in F). It can be seen that the IDDQ detection interval $[0, R^{10}_{Iddq}] \cup [R^{10}_C, R^{11}_{Iddq}]$ is non-contiguous. Moreover, it does not correspond to the interval $[0, R^{11}_{Iddq}]$ obtained by assuming the fault-free value (logic-1) in the flip-flop (as suggested in [9]). Hence, a defect with $R_{sh} \in [R^{10}_{Iddq}, R^{10}_C]$ would be incorrectly classified as detected.

As has been noted in [10], this behavior is unique for shorts with non-zero resistance. The analysis framework proposed in this paper is essential to identify the exact conditions under which the standard assumption is invalid. It would be impossible to derive this behavior without considering the short resistance explicitly.

4 Experimental Results

We applied 1,000 random test vectors to ISCAS 85 and combinational parts of ISCAS 89 (denoted as cs) benchmark circuits. The fault list consisted of 10,000 randomly selected non-feedback resistive shorts, where available. We selected 100 μA as the Delta-IDDQ threshold ΔI_{limit}. This is a typical resolution of high-current (> 100 μA) IDDQ measurement systems although better-resolving systems are also available. We did not observe much variability in results using ΔI_{limit} of 50 μA and even 10 μA. We employed the density function ρ derived from one used in [16] for all experiments. It is based on experimental data from [14] and assigns a lower probability to high-resistance defects, motivated by typical particle size distributions. All electrical parameters of the circuits are based on the 0.35 μm AMS (austriamicrosystems) technology. All measurements were performed on a 2GHz Linux machine with 1 GB RAM using the extended simulator from [11].

The goal of our experiments was to determine the detection capabilities of Delta-IDDQ testing alone and in combination with the conventional (voltage) testing. We reflected the fact that the number of IDDQ measurements is often lower than the number of voltage measurements, i.e., not every vector in the test set is used for an IDDQ measurement. For this purpose we performed three sets of experiments assuming that IDDQ is measured for 10, 100 or 1,000 out of the 1,000 applied vectors. Of special interest was the condition that a short defect *must not be activated for at least one vector* in order to ensure its detection. If only 10 IDDQ measurements are performed it is realistic that a short defect is activated (i.e., the involved nodes are set to the opposite logic values) for *every* of the measurement. Such a fault is missed by Delta-IDDQ testing because the reference value which consists of the background current level without a contribution of the defect to the overall current is missing. We studied the severity of this issue by calculating the number of shorts which were activated under all IDDQ measurements, called Always-Activated (AA) shorts, and excluding the detection of such shorts by IDDQ testing from the calculated coverages.

The results are summarized in Table 1. Average numbers are given in the bottom row of the table. The name

Circuit	FC^{logic}	Delta IDDQ, 10 measurements				IDDQ, 10 measurements		Delta IDDQ, 100 measurements				IDDQ, 100 measurements		Delta IDDQ, 1000 measurements				IDDQ, 1000 measurements	
		AA	FC^{Iddq}	FC^{Iddq}_{comb}	FC^{Iddq}_{flaw}	FC^{Iddq}	FC^{Iddq}_{comb}	AA	FC^{Iddq}	FC^{Iddq}_{comb}	FC^{Iddq}_{flaw}	FC^{Iddq}	FC^{Iddq}_{comb}	AA	FC^{Iddq}	FC^{Iddq}_{comb}	FC^{Iddq}_{flaw}	FC^{Iddq}	FC^{Iddq}_{comb}
c0432	99.78	53	97.60	100.00	97.58	98.62	100.00	0	100.00	100.00	99.96	100.00	100.00	0	100.00	100.00	99.96	100.00	100.00
c0499	99.99	2	92.81	100.00	92.03	92.84	100.00	0	96.70	100.00	95.86	96.70	100.00	0	100.00	100.00	99.11	100.00	100.00
c0880	98.88	167	96.27	99.91	96.18	97.94	99.94	8	99.82	99.96	99.73	99.90	99.96	0	99.98	99.98	99.89	99.98	99.98
c1355	99.89	170	95.99	99.93	95.93	97.70	99.93	89	97.92	99.94	97.85	98.81	99.94	0	100.00	100.00	99.93	100.00	100.00
c1908	99.25	88	98.07	99.93	96.79	98.97	99.93	45	99.30	99.97	98.00	99.76	99.97	27	99.71	99.98	98.40	99.98	99.98
c2670	95.93	120	97.41	99.93	97.31	98.61	99.96	6	99.94	100.00	99.87	100.00	100.00	5	99.95	100.00	99.88	100.00	100.00
c3540	99.19	172	95.58	99.91	95.13	97.31	99.93	26	99.71	100.00	99.24	99.97	100.00	25	99.75	100.00	99.28	100.00	100.00
c5315	99.96	34	99.21	100.00	99.15	99.55	100.00	5	99.95	100.00	99.89	100.00	100.00	5	99.95	100.00	99.89	100.00	100.00
c7552	99.12	39	99.08	99.98	99.00	99.47	99.98	1	99.98	100.00	99.90	99.99	100.00	1	99.99	100.00	99.91	100.00	100.00
cs00208	99.56	370	81.82	99.95	81.33	91.22	99.96	20	99.26	100.00	98.70	99.77	100.00	6	99.85	100.00	99.27	100.00	100.00
cs00298	99.98	42	98.31	100.00	97.83	99.26	100.00	8	99.80	100.00	99.31	99.98	100.00	7	99.84	100.00	99.35	100.00	100.00
cs00344	99.97	31	99.09	100.00	98.74	99.49	100.00	10	99.87	100.00	99.51	100.00	100.00	10	99.87	100.00	99.51	100.00	100.00
cs00349	99.97	37	99.01	100.00	98.65	99.49	100.00	10	99.87	100.00	99.52	100.00	100.00	10	99.87	100.00	99.52	100.00	100.00
cs00382	99.96	112	97.25	99.98	97.11	98.69	99.98	11	99.85	99.99	99.69	99.99	99.99	11	99.86	100.00	99.71	100.00	100.00
cs00386	99.82	226	91.60	99.97	91.61	94.04	99.97	26	99.43	100.00	99.37	99.71	100.00	0	100.00	100.00	99.94	100.00	100.00
cs00400	99.96	134	96.75	99.98	96.61	98.37	99.98	13	99.83	99.99	99.69	99.99	99.99	13	99.83	99.99	99.69	99.99	99.99
cs00420	85.20	896	82.17	96.14	81.87	91.20	96.21	368	92.75	97.01	92.47	96.45	97.03	244	95.27	97.71	95.01	97.72	97.72
cs00444	99.98	108	97.22	100.00	97.04	98.30	100.00	14	99.85	100.00	99.72	99.99	100.00	14	99.86	100.00	99.73	100.00	100.00
cs00510	99.98	371	92.80	100.00	92.78	96.52	100.00	2	99.97	100.00	99.97	99.99	100.00	0	100.00	100.00	100.00	100.00	100.00
cs00526	99.44	177	96.50	99.94	96.18	98.29	99.98	13	99.86	100.00	99.59	99.99	100.00	12	99.88	100.00	99.61	100.00	100.00
cs00641	99.61	80	98.22	99.97	98.02	99.02	99.98	14	99.84	100.00	99.64	99.98	100.00	14	99.86	100.00	99.66	100.00	100.00
cs00713	99.68	121	97.62	99.95	97.28	98.84	99.95	27	99.65	99.97	99.31	99.92	99.97	19	99.81	100.00	99.47	100.00	100.00
cs00820	96.29	334	93.99	99.77	93.75	97.37	99.86	13	99.83	99.98	99.68	99.96	99.98	9	99.91	100.00	99.76	100.00	100.00
cs00832	96.13	330	93.46	99.70	93.29	96.80	99.79	14	99.79	99.96	99.62	99.93	99.96	8	99.92	100.00	99.75	100.00	100.00
cs00838	69.83	1342	73.12	90.19	72.80	86.62	90.43	876	83.43	93.13	83.14	92.25	93.18	702	86.69	93.72	86.41	93.76	93.76
cs00953	97.33	1942	61.44	99.21	61.41	80.89	99.35	272	94.62	99.65	94.62	97.35	99.68	17	99.65	99.81	99.65	99.82	99.82
cs01196	96.07	486	88.88	99.06	88.88	93.75	99.19	18	99.56	99.89	99.53	99.74	99.89	1	99.99	100.00	99.96	100.00	100.00
cs01238	96.49	494	88	98.67	87.97	92.94	98.90	20	99.44	99.87	99.44	99.64	99.87	1	99.99	100.00	99.99	100.00	100.00
cs01423	99.21	77	97.57	99.94	97.06	98.35	99.96	2	99.91	99.99	99.38	99.93	99.99	0	100.00	100.00	99.47	100.00	100.00
cs01488	99.65	81	93.61	99.96	93.58	94.43	99.96	2	99.92	100.00	99.92	99.94	100.00	0	100.00	100.00	100.00	100.00	100.00
cs01494	99.66	115	92.98	99.96	92.92	94.14	99.97	3	99.95	100.00	99.90	99.98	100.00	0	100.00	100.00	99.95	100.00	100.00
cs05378	98.68	172	95.89	99.83	95.84	97.61	99.89	20	99.63	100.00	99.58	99.83	100.00	3	99.97	100.00	99.92	100.00	100.00
cs09234	90.92	188	95.98	99.24	95.88	97.87	99.50	66	98.67	99.62	98.57	99.34	99.68	19	99.67	99.82	99.57	99.86	99.86
cs13207	95.90	190	95.63	99.17	95.57	97.51	99.28	66	98.47	99.43	98.41	99.11	99.48	16	99.43	99.57	99.39	99.59	99.59
cs15850	96.76	161	96.33	99.58	96.29	97.94	99.76	27	99.23	99.90	99.20	99.50	99.92	1	99.96	99.97	99.93	99.97	99.97
cs35932	100.00	66	98.89	100.00	98.46	99.56	100.00	4	99.96	100.00	99.55	100.00	100.00	4	99.96	100.00	99.55	100.00	100.00
cs38417	97.73	92	98.09	99.84	98.08	99.01	99.90	6	99.83	99.96	99.82	99.89	99.96	2	99.96	99.98	99.95	99.98	99.98
cs38584	92.42	229	95.57	98.95	94.77	97.88	99.60	64	99.07	99.52	98.24	99.72	99.79	33	99.56	99.74	98.76	99.89	99.89
Average	97.32		93.68	99.44	93.44	96.48	99.50		98.80	99.68	98.56	99.39	99.69		99.42	99.74	99.18	99.75	99.75

Table 1: Fault coverages for Delta-IDDQ testing with 1000 test vectors for voltage testing, current threshold $\Delta I_{limit} = 100\mu A$ and different numbers of IDDQ measurements.

of the circuit is followed by the resistive short defect coverage of the voltage testing (without any IDDQ measurements), given for reference. Three sections given next report detailed results for 10, 100 and 1,000 IDDQ measurements, respectively. First, the number of Always-Activated faults (AA) is given. The coverage of Delta-IDDQ alone (FC^{Iddq}) and together with voltage testing (FC^{Iddq}_{comb}) follow. The coverage of flaws by IDDQ testing is contained in the next column (voltage testing cannot detect flaws by definition). Note that 10, 100 or 1,000 vectors are used for IDDQ testing while 1,000 vectors are always used for voltage testing. Any AA shorts detected by IDDQ measurements are not counted as detected for any resistance value while AA shorts detected by voltage testing are counted as detected because voltage testing is not invalidated for shorts which are always activated by every test.

It can be seen that the coverage by IDDQ testing alone is highly correlated with the number of AA shorts which it cannot detect. For circuits with few AA shorts the IDDQ coverage is very high even without support from voltage testing. On the other hand, the combination of IDDQ and voltage testing works very well even for very low number of IDDQ measurements. This is partly due to the fact that AA shorts are covered by voltage testing but not IDDQ testing. Moreover, it appears that IDDQ testing and voltage testing are orthogonal in the sense that IDDQ testing detects some of the defects missed by the voltage testing and vice versa. The coverage of flaws is also high.

In order to quantify the impact of AA shorts on the test quality, we generated data assuming that AA shorts are not eliminated from the list of the covered defects. The data are contained in the columns labelled "IDDQ" (rather than "Delta-IDDQ"). Note that these results are given mainly for reference and their physical meaning is limited. The numbers would have been correct if IDDQ (not Delta-IDDQ) had been employed. However, IDDQ testing with limit of only 100 μA does not appear realistic, as opposed to Delta-IDDQ. We ran experiments assuming a much higher threshold (up to 1,500 μA) more appropriate for regular (not Delta) IDDQ testing, and found that the test quality is reduced dramatically. The coverage obtained without elimination of AA short detections would also be realistic for Delta-IDDQ testing, if for every such short a vector which does *not* activate it were applied to the circuit. This could have been done by, e.g., using more random vectors or running a special ATPG. However, this would increase the test set size.

The additional results show that the coverage deterioration due to the AA vectors is significant. It is most severe if few IDDQ measurements are available (for 10 measurements, FC^{Iddq} changes from 93.68 to 96.48 on average depending on how the AA shorts are handled). This means that AA shorts needs to be accounted when estimating the quality of a test set. The results show that a sufficient number of IDDQ tests is required to achieve a high Delta-IDDQ fault coverage and that a limited IDDQ vector set does not meet this requirement. Also, the need for special test sets optimized to avoid AA shorts and ATPG tools to produce such test sets is obvious.

5 Conclusions

Delta-IDDQ is a technique which ensures meaningful application of IDDQ testing to large classes of state-of-the-art ICs. In this paper, we explored its detection capability for a relevant defect class, resistive shorts, using an advanced analytical model. In order to preserve realism, we accounted for specific limitations of Delta-IDDQ: we used only a subset of available vectors for IDDQ measurement, and we did not count detections of shorts which are activated by every test vector (Always-Activated shorts).

We showed that Delta-IDDQ provides excellent coverage of the considered defects, in particular in combination with voltage testing, if appropriate equipment sensitivity can be provided. This holds also for the coverage of flaws which are potential early-life failures. We found that the impact of the Always-Activated shorts is significant and that they must be addressed during both test set preparation and evaluation. Further, we demonstrated that some of the traditional assumptions for the sequential simulation of IDDQ effects are not valid for non-zero resistance shorts and that the proposed simulation technique still produces accurate results. Future work includes the consideration of the impact of process variations on the detection conditions.

6 References

[1] H. Manhaeve. Current testing for nanotechnologies: A demistifying application perspective. In *European Test Symp.*, pages 205–210, 2005. (Informal Proceedings).

[2] C. Thibeault. On the comparison of Delta Iddq and Iddq testing. In *VLSI Test Symp.*, pages 143–150, 1999.

[3] A. Fudoli, A. Ascagni, D. Appello, and H. Manhaeve. A practical evaluation of IDDQ test strategies for deep submicron production test application. experiences and targets from the field. In *European Test Workshop*, pages 65–70, 2003.

[4] H. Vierhaus, W. Meyer, and U. Glaser. CMOS bridges and resistive transistor faults: IDDQ versus delay effects. In *Int'l Test Conf.*, pages 83–91, 1993.

[5] R. Rodriguez-Montanes, J. Figueras, and A. Rubio. Current vs. logic testability of bridges in scan chains. In *European Test Conference 1993*, pages 392–396, 1993.

[6] M. Renovell, P. Huc, and Y. Bertrand. CMOS bridge fault modeling. In *VLSI Test Symp.*, pages 392–397, 1994.

[7] M. Renovell, P. Huc, and Y. Bertrand. The concept of resistance interval: A new parametric model for resistive bridging fault. In *VLSI Test Symp.*, pages 184–189, 1995.

[8] M. Renovell, F. Azaïs, and Y. Bertrand. Detection of defects using fault model oriented test sequences. *Jour. of Electronic Testing: Theory and Applications*, 14:13–22, 1999.

[9] P. Thadikaran, S. Chakravarty, and J. Patel. Fault simulation of I_{DDQ} tests for bridging faults in sequential circuits. In *Int'l Symp. on Fault-Tolerant Comp.*, pages 340–349, 1995.

[10] R. Rodrigues-Montanes and J. Figueras. Analysis of bridging defects in sequential CMOS circuits and their current testability. In *European Design and Test Conference*, pages 356–360, 1994.

[11] P. Engelke, I. Polian, M. Renovell, and B. Becker. Simulating resistive bridging and stuck-at faults. In *Int'l Test Conf.*, pages 1051–1059, 2003.

[12] P. Huc. *Test en tension des courts-circuits en technologie CMOS*. PhD thesis, Université de Montpellier II Sciences et Techniques du Languedoc, Montpellier, France, March 1995.

[13] I. Polian, S. Kundu, J.M. Galliere, P. Engelke, M. Renovell, and B. Becker. Resistive bridge fault model evolution from conventional to ultra deep submicron technologies. In *VLSI Test Symp.*, pages 343–348, 2005.

[14] R. Rodríguez-Montañés, E.M.J.G. Bruls, and J. Figueras. Bridging defects resistance measurements in a CMOS process. In *Int'l Test Conf.*, pages 892–899, 1992.

[15] M. Spica, M. Tripp, and R. Roeder. A new understanding of bridge defect resistances and process interactions from correlating inductive fault analysis predictions to empirical test results. In *IEEE Int'l Workshop on Current and Defect-Based Testing*, pages 11–16, 2001.

[16] C. Lee and D. M. H. Walker. PROBE: A PPSFP simulator for resistive bridging faults. In *VLSI Test Symp.*, pages 105–110, 2000.