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Design of an Optimal Test Pattern Generator for Built-in Self Testing of Path Delay Faults

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Abstract

A novel design of an optimal test pattern generator (TPG) for built in self testing of path delay faults is presented. For delay testing in an n-input CUT, the proposed TPG generates a sequence S of length $n \cdot 2^n + 1$ that includes all $n \cdot 2^n$ single-input-change (SIC) test patterns, and hence optimal. Generation of such a sequence of minimum length was an open problem. We establish existence of such a sequence from the presence of an eulerian trail in a bi-directional boolean cube. A recursive technique of generating S is then proposed using a novel structure called complementation sequence tree. Finally, a simple iterative design of a TPG is proposed, which can be cascaded to form larger generators for any value of n. The TPG provides minimum test application time for testing path delay faults with SIC two-pattern tests.

Gastgeber: Prof. Dr. Bernd Becker

Alle Interessenten sind recht herzlich eingeladen.

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