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IDDQ Test Compaction for Sequential Circuits

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Abstract

In this talk we will present two methods to reduce IDDQ testing time for sequential circuits. One method is to reduced a given test sequence directly and the other is to select IDDQ measurement vectors among the sequence. The basic idea of the first method is to remove redundant test vectors by using reassignment method, which is to apply the backtrace procedure for a detected fault in order to introduce don't care values. If don't care values appear in all flip-flops, then the vector corresponding to this time frame can be deleted. Second method is to reduce the number of IDDQ measurement vectors by fault simulation to form a detection matrix, for which measurement test vectors can be selected by solving a minimum set cover problem. In this fault simulation the effect of bridging faults must be considered to reflect the correct selection of measurement vectors. Experimental results for these methods show that test sequences generated by weighted random vectors can be reduced to short sequences with less computation time.

Gastgeber: Prof. B.Becker

Alle Interessenten sind recht herzlich eingeladen.

Organisation : Prof. Dr. B. Becker / F. Schmiedle

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