Versuchsbeschreibung Nr. 3

<u>Verwendete Geräte:</u> 1 Oszilloskop 2 Multimeter

<u>Literatur:</u>
1. Tietze,Schenk: Halbleiterschaltungstechnik (Kap. 2.1,2.2,7,8.5,14.3)
2. Beuth Bauelemente (Kap. 9.6)

<u>Teil 1:</u>
- Kennenlernen von RC- und CR-Gliedern
- Tiefpass / Hochpass

<u>Aufgaben:</u>

1. Von der folgenden Schaltung soll C berechnet werden, so daß die Spannung u_a am Ausgang nach 50μs auf 10 % der Eingangsspannung u_e abgeklungen ist.

Eingangsspannung:
- Kurvenform: Rechteck
- Amplitude: $V_{ss} = 5V$ (Offset so, daß Rechteck von 0 - 5V geht)
- Frequenz: 100Hz

- Verwenden Sie für diesen Versuch Kunststoffkondensatoren.
- Stellen Sie u_a am Oszi dar, und nehmen Sie das Zeitverhalten auf.
- Messen Sie mit der Menüfunktion Cursor die vorgegebenen Werte nach.
- Speichern der Meßung im folgenden Directory als BMP-Bild **c:\labor\vers3\a1_bild1.bmp**
- Drucken Sie das Zeitverhalten mit der Oszisoftware "Oszi" unter Windows aus.
- Verändern Sie die Frequenz von u_e, und beobachten Sie u_a !
- Was passiert, wenn Sie C und R vertauschen ?
- Beschreiben Sie die Funktionalität von RC- bzw. CR-Gliedern ?

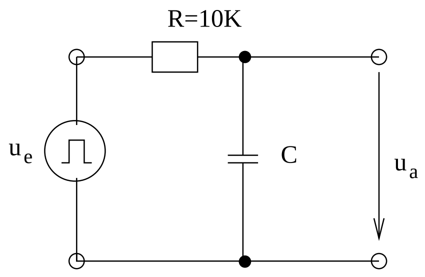


Abb.5: Schaltung zur Messung des Verhaltens eines RC-Gliedes

Teil 2: - Operationsverstärkerschaltungen

Bei dem in diesem Versuch verwendeten Operationsverstärker handelt es sich um den TL082, dessen Datenblatt im Anhang zu finden ist.

Für diesen Versuchsteil steht ein Versuchsbrett zur Verfügung, das für die jeweilige Aufgabe umgebaut werden muß. Im Anhang finden sich nähere Erläuterungen zum Versuchsbrett.

Aufgaben:

2. Entwerfen Sie einen invertierenden Vertsärker für

a) V = 1
b) V = 2
c) V = 3

- Bauen Sie die Schaltung mit dem für die nächsten drei Aufgaben zur Verfügung stehendem Versuchskasten auf. Die Versorgungsspannung des Operationsverstärkers beträgt VCC = +15V , VEE = -15V und 0V. (In-Reiheschalten der Netzgeräte !)
- Verwenden Sie als Eingangsspannung eine Sinusspannung ohne Offset.
- Kontrollieren Sie die Verstärkungen, in dem Sie jeweils Aus- und Eingangsspannung mit dem Oszilloskop aufzeichnen.
- Speichern Sie die Meßaufnahmen im folgenden Directory als BMP-Bilder **c:\labor\vers3\a2_bild1.bmp und a2_bild2.bmp und a2_bild3.bmp** und drucken Sie die Meßaufnahmen mit der Oszisoftware aus.

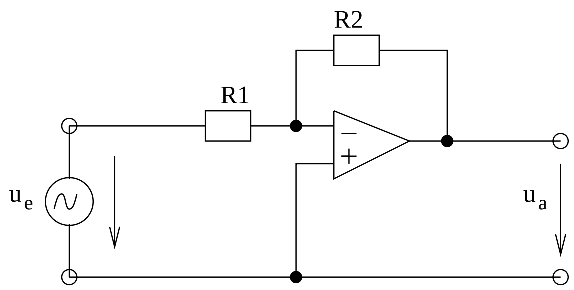


Abb.6: Invertierender Verstärker

3. Entwerfen Sie eine Tiefpass für ein Gleichspannungsverstärkung von 5 und eine Grenzfrequenz von 400 Hz.

Kontrollieren Sie das Tiefpassverhalten durch Aufnahme des Frequenzganges, und tragen Sie diesen in halblogarithmisches Papier ein.

Formeln zur Berechnung eines Tiefpasses:

$R \cdot C = \frac{1}{2 \cdot \pi \cdot f_g}$

Gleichspannungsverstärkung: $V = -\frac{R_2}{R_1}$

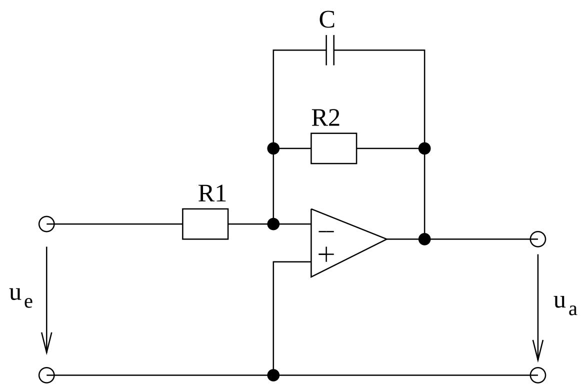


Abb.7: Tiefpass mit Operationsverstärker (OP)

4. Legen Sie an den nichtinvertierenden Eingang des Operationsverstärkers +5V an, wie in Abb.8 zu sehen ist.

Legen Sie nun an den invertierenden Eingang nacheinander folgende Eingangsspannungen an:

Eingangsspannung:

- Kurvenform: a)Rechteck b) Sinus c) Sägezahn
- Frequenz: 1 KHz

Die Versorgungsspannung des Operationsverstärkers beträgt
VCC = +10V , VEE = -10V und 0V.

Verändern Sie die Amplitude der Eingangsspannung, um zu sehen, welchen Effekt dies auf die Ausgangsspannung hat, und beschreiben Sie das Verhalten des Operationsverstärkers.

Speichern sie günstige Meßaufnahmen im folgenden Directory als BMP-Bilder
c:\labor\vers3\a4_bild1.bmp, a4_bild2.bmp, a4_bild3.bmp und
drucken Sie die entsprechenden Meßaufnahmen mit der Oszisoftware "Oszi" unter Windows aus.

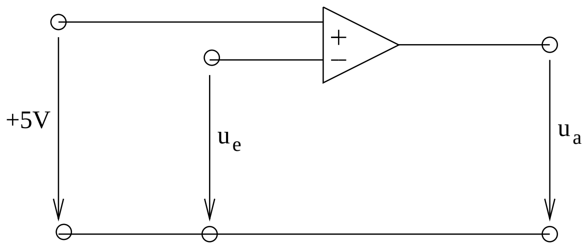


Abb.8: Meßschaltung zu Aufgabe 4

National Semiconductor

November 1994

TL082 Wide Bandwidth Dual JFET Input Operational Amplifier

TL082 Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

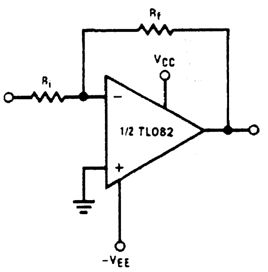
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

■ Internally trimmed offset voltage	15 mV
■ Low input bias current	50 pA
■ Low input noise voltage	$16 nV/\sqrt{Hz}$
■ Low input noise current	$0.01 pA/\sqrt{Hz}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	$13 V/\mu s$
■ Low supply current	3.6 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20 Vp - p$, BW = 20 Hz–20 kHz	$<0.02\%$
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	$2 \mu s$

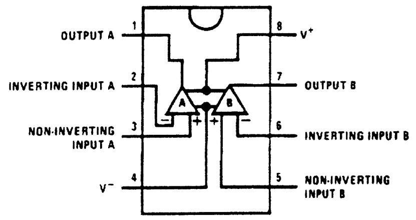
Typical Connection



TL/H/8357-1

Connection Diagram

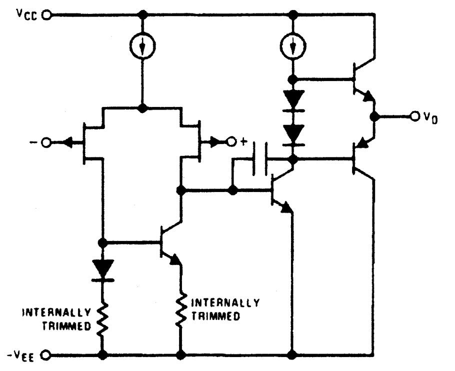
DIP/SO Package (Top View)



TL/H/8357-3

Order Number TL082CM or TL082CP
See NS Package Number M08A or N08E

Simplified Schematic



TL/H/8357-2

BI-FET II™ is a trademark of National Semiconductor Corp.

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RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 1)
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$ Over Temperature		5	15 20	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$		10		$\mu V/°C$
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 4, 5) $T_j \leq 70°C$		25	200 4	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 4, 5) $T_j \leq 70°C$		50	400 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2\ k\Omega$ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	70	100		dB
I_S	Supply Current			3.6	5.6	mA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1Hz-20 kHz (Input Referred)		−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	8	13		$V/\mu s$
GBW	Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1000 Hz		25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, f = 1000 Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 115°C/W junction to ambient for the N package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: The power dissipation limit, however, cannot be exceeded.

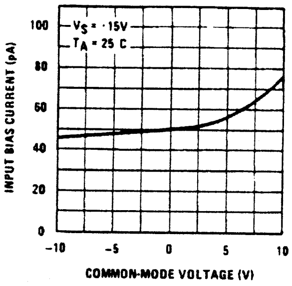
Note 4: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

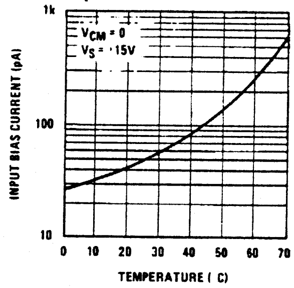
Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. $V_S = \pm 6V$ to $\pm 15V$.

Typical Performance Characteristics

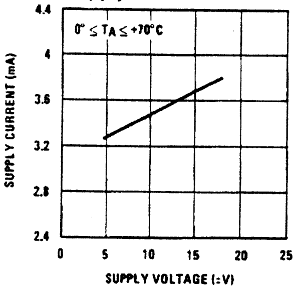
Input Bias Current



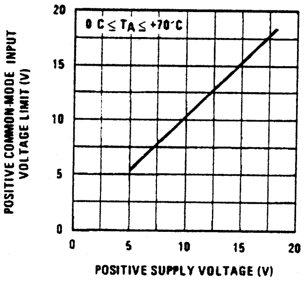
Input Bias Current



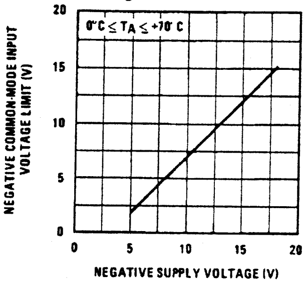
Supply Current



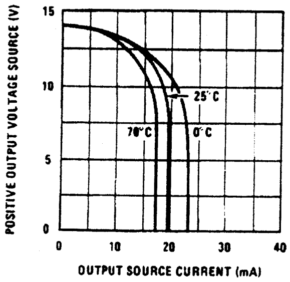
Positive Common-Mode Input Voltage Limit



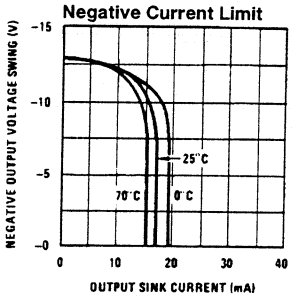
Negative Common-Mode Input Voltage Limit



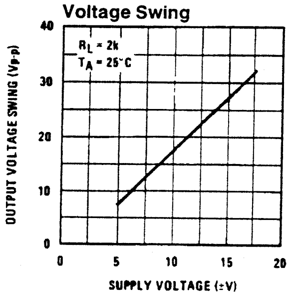
Positive Current Limit



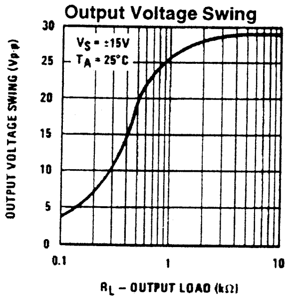
Negative Current Limit



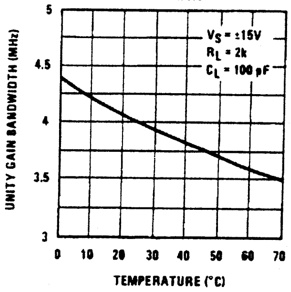
Voltage Swing



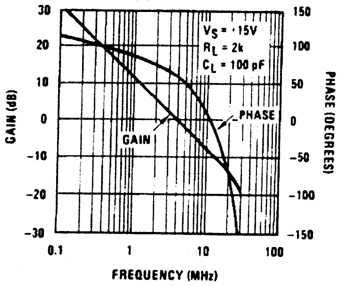
Output Voltage Swing



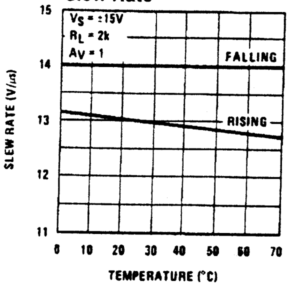
Gain Bandwidth



Bode Plot



Slew Rate



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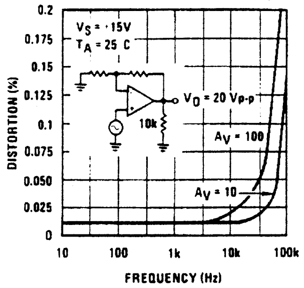
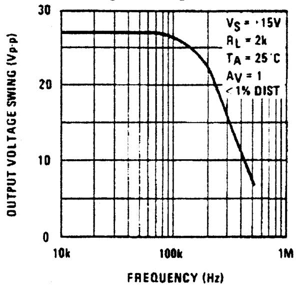
Typical Performance Characteristics (Continued)

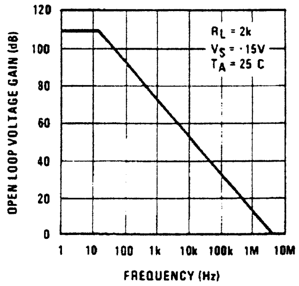
Distortion vs Frequency



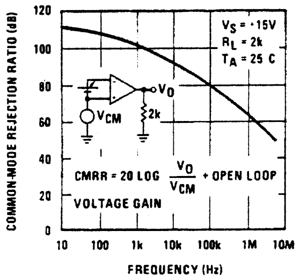
Undistorted Output Voltage Swing



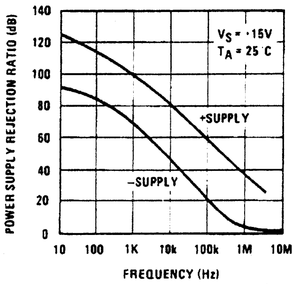
Open Loop Frequency Response



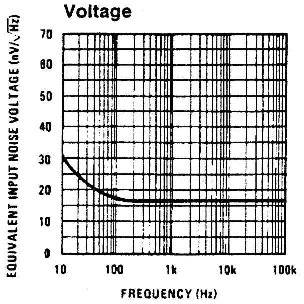
Common-Mode Rejection Ratio



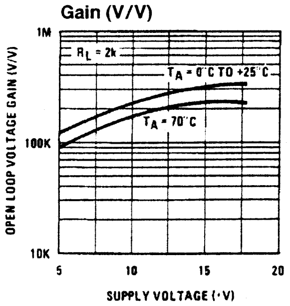
Power Supply Rejection Ratio



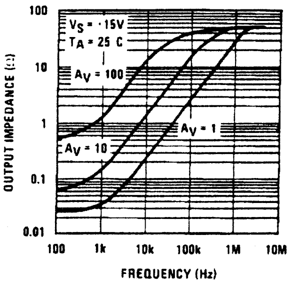
Equivalent Input Noise Voltage



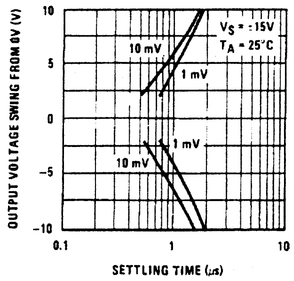
Open Loop Voltage Gain (V/V)



Output Impedance



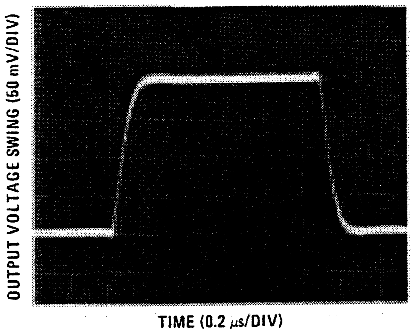
Inverter Settling Time



TL/H/8357–5

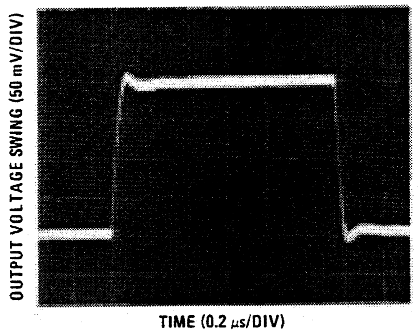
Pulse Response

Small Signal Inverting



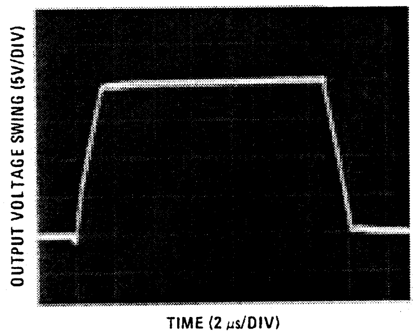
TL/H/8357-6

Small Signal Non-Inverting



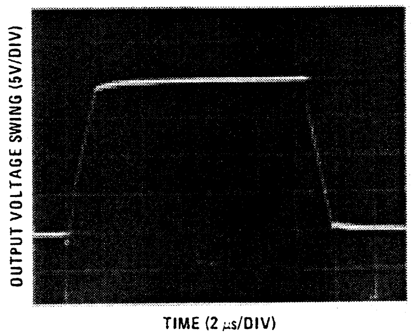
TL/H/8357-7

Large Signal Inverting



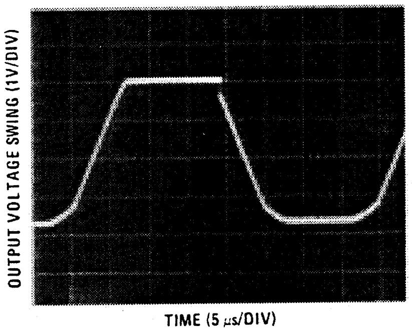
TL/H/8357-8

Large Signal Non-Inverting



TL/H/8357-9

Current Limit (R_L = 100Ω)



TL/H/8357-10

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case

Application Hints (Continued)

does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

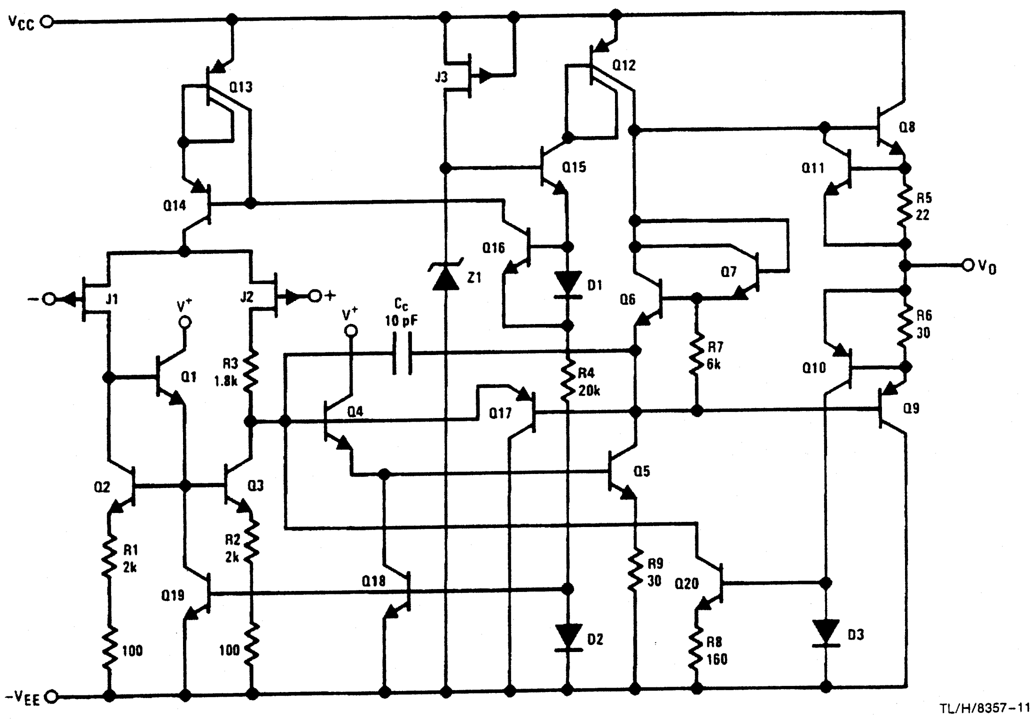
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

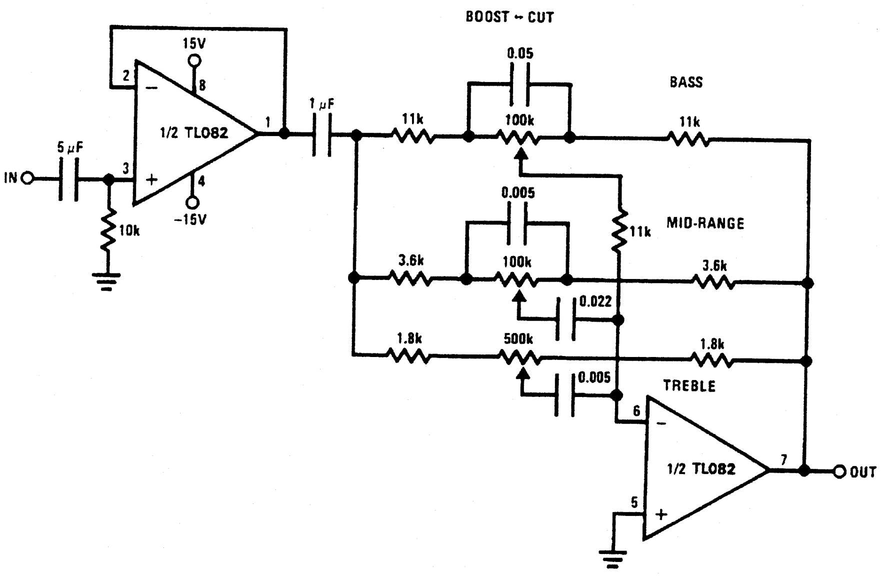
Detailed Schematic



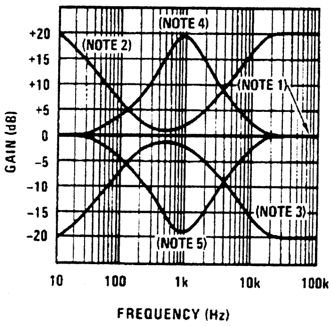
TL/H/8357-11

Typical Applications

Three-Band Active Tone Control



TL/H/8357-12



TL/H/8357-13

Note 1: All controls flat.

Note 2: Bass and treble boost, mid flat.

Note 3: Bass and treble cut, mid flat.

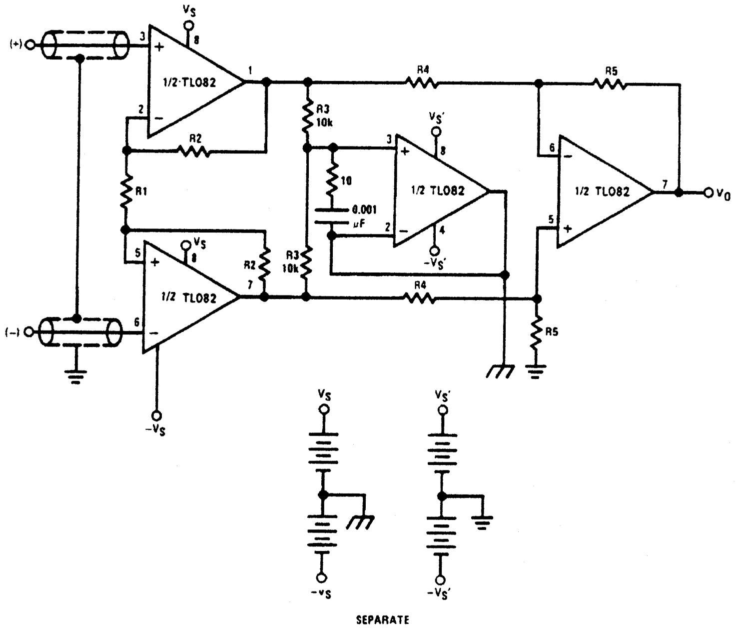
Note 4: Mid boost, bass and treble flat.

Note 5: Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier



TL/H/8357-14

$$A_V = \left(\frac{2R2}{R1} + 1\right)\frac{R5}{R4}$$

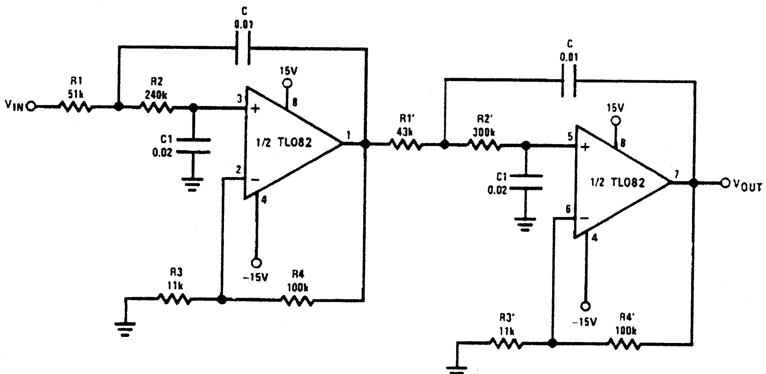
and are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With A_{V_T} = 1400, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

Fourth Order Low Pass Butterworth Filter

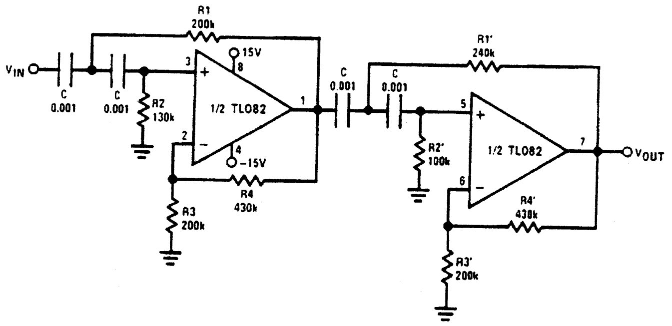


TL/H/8357-15

- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

Typical Applications (Continued)

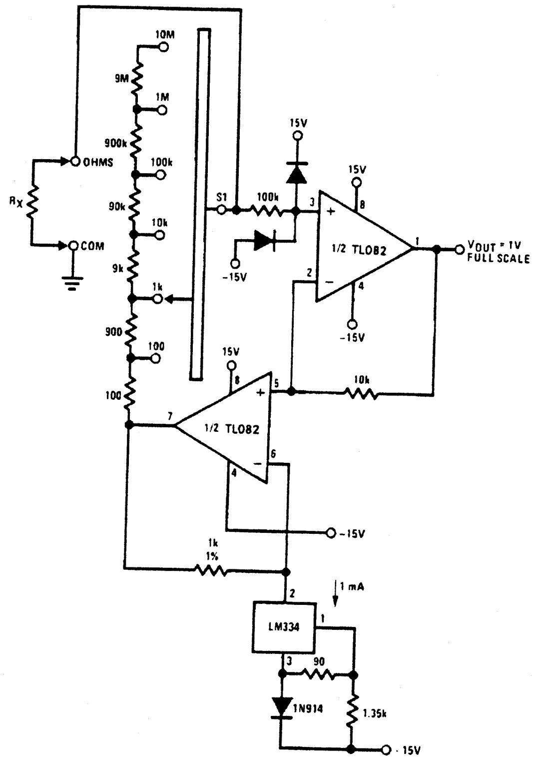
Fourth Order High Pass Butterworth Filter



TL/H/8357-16

- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2C^2}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

Ohms to Volts Converter

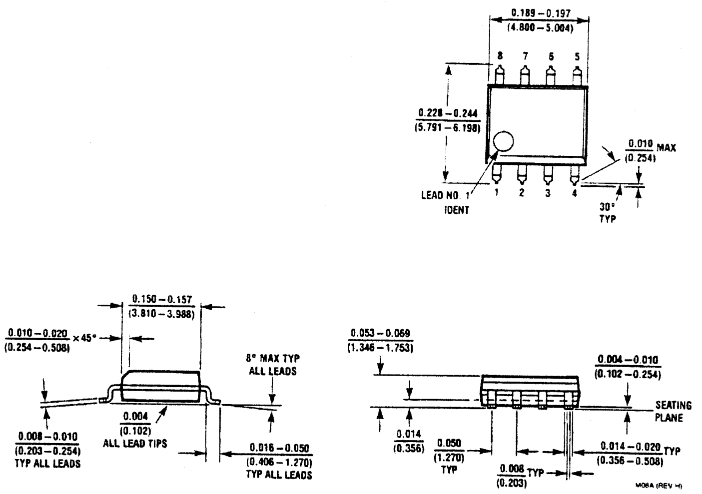


TL/H/8357-17

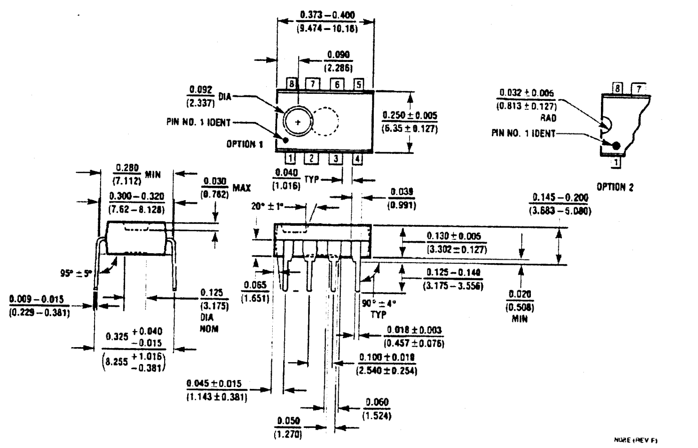
$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 7 of the TL082CP.

Physical Dimensions inches (millimeters)



Order Number TL082CM
NS Package M08A



Order Number TL082CP
NS Package N08E

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Erläuterungen zum Versuchskasten Operationsverstärker

Der Versuchskasten zum Operationsverstärker ist so aufgebaut, daß möglichst wenig selbst aufgebaut werden muß.

Der Baustein TL082 enthält 2 Operationsverstärker, von denen nur der linke verwendet wird.

Um zusätzliche Bauteile und Drähte stecken zu können sind Buchsenleisten an den Baustein angeschlossen, wie auf der nächsten Seite abgebildet ist.

Die dicken schwarzen Striche stellen die schon vorhandene Verdrahtung da.

Der Eingang und Ausgang des Operationsverstärkers muß auch nicht mehr seperat verdrahtet werden, sie sind auf die BNC-Buchsen am Rand des Versuchsbrettes geführt.

Die Versorgung für den Operationsverstärker wird per Leitung an die Buchsen VCC (= 15V), GND (= 0V) und VEE (= -15V) angeschlossen.

Der 5-V-Anschluß wird für den letzten Versuchsteil benötigt.

Abbildung des Versuchskasten Operationsverstärker