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Testability of AND/EXOR Expressions

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Abstract

It is often stated that AND/EXOR circuits are much easier testable than AND/OR circuits. In this paper we show that this is not true for all 2-level circuits based on EXOR. The statement only holds for restricted classes of AND/EXOR expressions, like Positive Polarity Reed-Muller Expressions and Fixed Polarity Reed-Muller Expressions. AND/EXOR circuits are studied with respect to deterministic and random pattern testability. We present experimental results that show that in general minimized 2-level AND/OR circuits are as well (or badly) testable as minimized 2-level AND/EXOR circuits.

1 Introduction

Many papers on AND/EXOR minimization use as a motivation that AND/EXOR circuits are much better testable than AND/OR circuits (see e.g. [21, 15, 1, 8, 10]).

This results from the observation that good *Deterministic Testability* (DT) properties can be proven for circuits derived from restricted classes of *Exclusive-or Sum-Of-Products expressions* (ESOPs) like *Positive Polarity Reed-Muller Expressions* (PPRMs) [12] and *Fixed Polarity Reed-Muller Expressions* (FPRMs) [15]. For PPRM circuits also good *Random Pattern Testability* (RPT) results have been proven [9].

In this paper we point out that the result of [9] can be extended to FPRM circuits. For larger classes of AND/EXOR circuits analogous results are not proven - nor for DT neither for RPT. In contrast, we show by experimental results that testability of minimized 2-level AND/EXOR circuits is similar to testability of minimized 2-level AND/OR circuits, which have already been shown to be quite badly testable in [22]. In our experiments we consider different realizations of EXOR gates with more than two inputs, i.e. they are realized by a cascade or a balanced tree of 2-input EXOR gates. Furthermore, we also examine a combination of both realizations. Additionally, the effect of considering each 2-input EXOR gate as a basic cell or substituting it by a 4-NAND realization is shown.

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2 Preliminaries

In this section basic notations are introduced which are important for the understanding of the paper.

2.1 Exclusive-or Sum-Of-Products Expressions

For *Exclusive-or Sum-Of-Products expressions* (ESOPs) various restricted subclasses can be considered. In the following we use the notations from [20]. To make the paper self-contained we review the main notations. (For more details see [17, 20].)

A Boolean function $\mathbf{B}^n \to \mathbf{B}$ can be decomposed by the following formulae:

$$\begin{aligned} f &= \overline{x}_i f_i^0 \oplus x_i f_i^1 && \textit{Shannon } (S) \\ f &= f_i^0 \oplus x_i f_i^2 && \textit{positive Davio } (pD) \\ f &= f_i^1 \oplus \overline{x}_i f_i^2 && \textit{negative Davio } (nD) \end{aligned}$$

f_i^0 (f_i^1) denotes the *cofactor* of f with respect to $x_i = 0$ ($x_i = 1$) and f_i^2 is defined as $f_i^2 := f_i^0 \oplus f_i^1$, $\oplus$ being the EXOR operation.

Depending on the restriction which formulae can be applied different classes of expressions can be defined:

Positive Polarity Reed-Muller Expression (PPRM): Only pD decomposition is applied.

Fixed Polarity Reed-Muller Expression (FPRM) [13]: Only pD and nD decomposition is applied with the restriction that each variable has a fixed decomposition type.

Kronecker Expression (KRO) [4]: pD, nD and S decomposition is applied with the restriction that each variable has a fixed decomposition type.

Reduced KRO (KRO) [5]: If in KROs the S decomposition is applied and both resulting subfunctions represent the same Boolean function the expression can easily be simplified [5]. The resulting 2-level expression is called an RKRO.

Pseudo Kronecker Expression (PSDKRO) [4]: pD, nD and S decomposition is applied. To each subfunction again all possible decompositions are applied until constant functions are obtained.

In the following we restrict ourselves to the following four AND/EXOR classes: PPRM, FPRM, RKRO, ESOP. They include the most restricted and the most general class, i.e. PPRM and ESOP and additionally two of the "inner classes".

2.2 Fault Model

A circuit can be viewed as a directed acyclic graph whose vertices are labeled with a basic cell type (AND, OR, NAND, NOR, EXOR, INVERTER) or with the name of a *Primary Input* (PI) or a *Primary Output* (PO).

The fault model adopted in this paper is the *Stuck-At Fault Model* (SAFM) [7, 3] that is well-known and used throughout the industry. It verifies the logical behavior of the circuit. We use the single-fault assumption, i.e., we assume that at most one fault can occur in the circuit.

Definition 1 A *single stuck-at fault* causes exactly one input or output pin of a node in the circuit C to have a fixed constant value (0 or 1) independently of the values applied to the PIs of the circuit.

An input vector I to C is a *test* for a stuck-at fault F, iff the values of the POs of C on applying I to the PIs in the presence of F are different from the values of the POs of C in the fault free case.

3 Testability of AND/EXOR Expressions

In this section we review the main results proven for testability of AND/EXOR expressions (see also [19]). We extend a theoretical result on RPT for PPRMs to FPRMs.

3.1 Deterministic Testability

For PPRM circuits a modification was presented in [12] which allows to test the circuits for the single SAFM with only $n + 4$ input vectors. The *modified PPRM circuits* need one extra input and one extra output. This result was extended to multi-faults in [14].

The generalization of [12] to FPRM circuits was given in [15]. The extension of [14] to FPRM circuits is straightforward. Motivated by these results it has often been stated that AND/EXOR circuits are easily testable. But the results have only been proven for the very restricted classes of PPRM and FPRM circuits.

The major drawback of these easily testable circuits is their size: There exist several functions that have only exponentially sized PPRMs and FPRMs, but can be represented by small ESOPs [18].

3.2 Random Pattern Testability

RPT for AND/EXOR circuits has only been studied in [9]. There, it has been shown that for modified PPRM ciruits [12] a weighted random pattern test with expected length of $O(n \cdot \log(n))$ exists to test all faults in the single SAFM. In the following we show

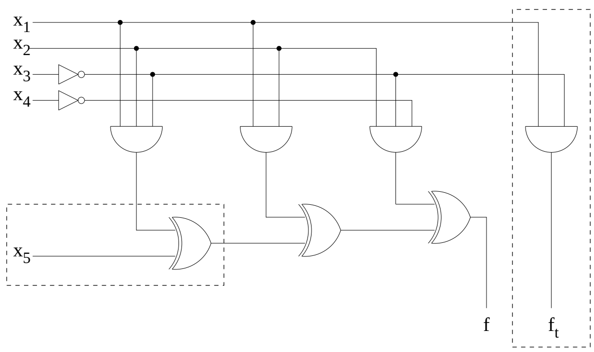

Figure 1: Modified FPRM circuit

that this result can also be extended to FPRMs. The modifications proposed in [12] for PPRM circuits can be adapted to FPRM circuits.

Example 1 The modified FPRM circuit for the function $f(x_1, x_2, x_3, x_4) = x_1x_2\overline{x}_3 \oplus x_1x_2 \oplus x_2\overline{x}_3\overline{x}_4$ is given in Figure 1. Dashed boxes are used to identify the extra hardware for testing purposes. During normal operation 0 must be applied to the test input x_5.

Theorem 1 For each Boolean function $f : \{0,1\}^n \rightarrow \{0,1\}$ a probability distribution P_r for the input probabilities exists such that the expected test length to test all single stuck-at faults in the modified FPRM circuit is $O(n \cdot \log(n))$.

Proof: The proof of the theorem can be performed analogously to [9]. Here, we only show which input vectors can be used to test all single stuck-at faults and how the probability distribution for the inputs of the FPRM circuit have to be chosen to get a short expected test length.

The PIs of the FPRM circuit are denoted by $x_1, x_2, \ldots, x_n$. If the variable x_i is decomposed by pD and therefore the variable x_i appears in the corresponding FPRM only in uncomplemented form then the polarity $p_i = 1$. If x_i is decomposed by nD and therefore only the complemented variable $\overline{x}_i$ is used in the FPRM then the polarity $p_i = 0$. The extra test input is called x_{n+1}. The input vectors t_i^ϵ ($i \in \{1, 2, \ldots, n+1\}$; $\epsilon \in \{0,1\}$) are defined as follows:

$$t_i^\epsilon(x_j) = \begin{cases} p_j & if \quad j \neq i \ \wedge \ j \leq n \\ \overline{p}_j & if \quad j = i \ \wedge \ j \leq n \\ \epsilon & if \quad j = n+1 \end{cases}$$

The probability distribution P_r defines for each PI x_i ($i \in \{1, 2, \ldots, x_{n+1}\}$) the probability that value 1 is assumed for a random input vector. The values for P_r are chosen analogously to [9]:

$$P_r(x_i) = \begin{cases} (n-1)/n & if \quad p_i = 1 \wedge j \leq n \\ 1/n & if \quad p_i = 0 \wedge j \leq n \\ 1/2 & if \quad j = n+1 \end{cases}$$

Then the probability for each of the $2n+2$ input vectors[1] t_i^ϵ ($i \in \{1, 2, \dots, n+1\}$; $\epsilon \in \{0, 1\}$) is given by:

$$\begin{aligned} P_r(t_i^\epsilon) &= \prod_{j=1}^{n+1} P_r(x_j) \cdot t_i^\epsilon(x_j) + (1 - P_r(x_j) \cdot \overline{t}_i^\epsilon(x_j) \\ &\geq \frac{1}{2} \cdot \left(\frac{n-1}{n}\right)^{n-1} \cdot \frac{1}{n} \end{aligned}$$

These probabilities are equal to the probabilities of the $2n+2$ input vectors used in [9] and therefore the expected test length to generate all input vectors t_i^ϵ is also bounded by $O(n \cdot \log(n))$. □

Thus, it has been proven that RPT of FPRM circuits is as good as RPT of PPRM circuits.

4 Experimental Results

In this section we present experimental results. All experiments have been carried out on a *Sun Sparc 1+* workstation.

In the following we compare DT and RPT of circuits derived from various classes of ESOPs with circuits derived from *Sum-Of-Products expressions* (SOPs). For minimization we used the following minimizers: [6] for PPRMs and FPRMs, [5] for RKROs, [11] for ESOPs, and [2] for SOPs.

Before we consider the testability of the circuits, we give an impression of their sizes. The number of terms needed for each benchmark is given in Table 1[2]. *in* (*out*) denotes the number of inputs (outputs) of the function. (A dash symbolizes that the resulting expression has more than 4000 terms.)

4.1 Deterministic Testability

In a first series of experiments we examined different realizations of EXOR gates with more than two inputs. On the one hand we use a cascade (C) of 2-input EXOR gates. On the other hand we consider a tree-like (T) realization [19], since the resulting circuits have smaller depth and as a result are faster. We also combined cascade and trees (CT), by grouping eight inputs that are realized by a tree and the groups are cascaded. The modification presented by Reddy in [12] (see also Example 1) is denoted by CR.

Since DT has only been considered theoretically for PPRM and FPRM circuits we also restrict ourselves to these two classes. The fault coverages obtained by applying the $n+4$ input vectors proposed in [12, 15] are given in Tables 2 and 3. In Table 2 2-input EXOR gates are considered to be a basic cell type and in Table 3 each EXOR gate is substituted by a 4-NAND realization. Only CR circuits are fully testable. Testability of most T and CT circuits is worse than that of the C and CR circuits. For circuit *cps* DT of T and CT circuits is even less than 90%. Comparing the results of Table 2 and Table 3 it can be seen that the fault coverage is significantly decreased by substituting the basic EXOR cells by 4-NAND realizations. This effect has been examined in more detail.

The number of redundancies for different realizations of the circuit *add6* are given in Table 4[3]. Besides considering the EXOR cell as a basic cell type we used the 4-NAND realization and the AND/OR/INVERTER realization for the EXOR. There are no redundancies for all classes of circuits if the EXOR is considered to be a basic cell type. Also for the modified PPRM and FPRM circuits there are no redundancies. This is because the modifications are made in such a way, that every cellular fault [3] can be tested at the EXOR cells and therefore every non-redundant realization of the EXOR cell cannot cause redundancies in the circuits. For all other types of AND/EXOR circuits there are redundancies, while the AND/OR circuits have no redundancies, independant of the way the EXOR gates with more than two inputs are realized. This observation is the same for all other benchmarks, i.e. if the EXOR gates are substituted the resulting circuits have many redundancies.

4.2 Random Pattern Testabilty

In this subsection we consider RPT of circuits derived from FPRMs, RKROs, ESOPs and SOPs. PPRM circuits are left out, since most of the larger circuits cannot be represented as PPRMs in reasonable size and for the remaining circuits testability is very similar to FPRM circuits (see Subsection 3.2). Each EXOR gate is substituted by a 4-NAND realization to make a fair comparison to SOP circuits. (If EXOR gates are allowed the RPT of AND/EXOR circuits is slightly improved by about 2% on average, but the overall results remain the same.)

1000 randomly generated input vectors are applied to each circuit. In Table 5 the resulting fault coverages are given. Here, we only consider the classes C and T, since no obvious extension of CR for SOP and ESOPs exists and since CT and T have about the same testability properties.

The experiments show that AND/OR circuits are often better testable with random patterns than AND/EXOR circuits. In contrast, FPRM circuits have often better RPT properties than AND/OR circuits - although we have not used weighted random patterns - but often lead to larger circuits.

[1] It is also possible to test all faults in the single SAFM for modified FPRM circuits with only $n+4$ input vectors [16]. But the presented $2n+2$ patterns are better suited to be generated by weighted random patterns with only one probability distribution [9].

[2] For all considered benchmarks where the PPRM could be constructed the minimized FPRM actually was a PPRM.

[3] Since for KROs, ESOPs and SOPs no extension with respect to [12] exist, these entries are marked with '*'.

name	*in*	*out*	PPRM	FPRM	RKRO	ESOP	SOP
add6	12	7	132	132	132	127	355
addm4	9	8	160	160	119	89	199
bc0	26	11	-	1117	349	168	179
cps	24	109	-	291	183	135	163
gary	15	11	-	349	246	96	107
in7	26	10	-	68	48	35	54
mlp4	8	8	97	97	85	63	128
rd53	5	3	20	20	20	15	31
rd73	7	3	63	63	63	36	127
vg2	25	8	-	-	398	184	110

Table 1: Number of terms for minimized benchmarks

name	PPRM				FPRM			
	C	T	CT	CR	C	T	CT	CR
add6	100	98.98	99.49	100	100	98.98	99.49	100
addm4	100	100	99.95	100	100	100	99.95	100
bc0	-	-	-	-	99.94	99.80	99.73	100
cps	-	-	-	-	99.39	99.27	99.21	100
gary	-	-	-	-	99.89	99.87	99.80	100
in7	-	-	-	-	98.28	98.50	98.07	100
mlp4	100	100	99.92	100	100	100	99.52	100
rd53	99.25	99.25	99.25	100	99.25	99.25	99.25	100
rd73	99.80	99.80	100	100	99.80	99.80	100	100
vg2	-	-	-	-	-	-	-	-

Table 2: Deterministic testability with EXOR gates

name	PPRM				FPRM			
	C	T	CT	CR	C	T	CT	CR
add6	96.86	92.52	94.87	100	96.86	92.52	94.87	100
addm4	98.57	96.34	95.96	100	98.57	96.34	95.96	100
bc0	-	-	-	-	98.60	93.04	93.15	100
cps	-	-	-	-	92.33	89.40	89.15	100
gary	-	-	-	-	96.90	93.82	93.47	100
in7	-	-	-	-	91.82	92.58	90.65	100
mlp4	98.72	95.93	95.37	100	98.72	95.93	95.37	100
rd53	92.17	91.15	93.87	100	92.17	91.15	93.87	100
rd73	94.44	93.80	94.89	100	94.44	93.80	94.89	100
vg2	-	-	-	-	-	-	-	-

Table 3: Deterministic testability without EXOR gates

	EXOR				4-NAND				AND/OR/INVERTER			
	C	T	CT	CR	C	T	CT	CR	C	T	CT	CR
PPRM	0	0	0	0	15	3	9	0	10	2	6	0
FPRM	0	0	0	0	15	3	9	0	10	2	6	0
RKRO	0	0	0	*	33	96	96	*	22	64	64	*
ESOP	0	0	0	*	45	93	92	*	28	59	58	*
SOP	0	0	0	*	0	0	0	*	0	0	0	*

Table 4: Number of redundancies for circuit add6

name	FPRM		RKRO		ESOP		SOP	
	C	T	C	T	C	T	C	T
add6	98.89	99.78	97.79	96.43	95.72	94.65	85.72	84.30
addm4	99.03	97.53	96.26	95.08	92.35	90.84	97.84	97.80
bc0	83.52	78.33	70.46	67.65	77.40	75.48	81.04	80.51
cps	62.80	54.78	47.85	43.30	50.74	50.44	38.35	39.05
gary	85.17	80.94	83.47	81.78	72.10	70.97	72.72	72.08
in7	81.76	80.72	76.61	75.45	70.78	68.78	74.04	74.26
mlp4	99.28	97.20	96.77	94.59	92.58	90.67	99.62	99.62
rd53	96.93	96.93	94.40	93.47	92.44	94.18	100	100
rd73	98.63	98.08	97.43	95.12	97.97	95.94	100	100
vg2	-	-	68.31	67.23	64.10	60.67	73.40	73.10

Table 5: Random pattern testability

5 Conclusions

In this paper deterministic and random pattern testability has been considered for circuits derived from different classes of 2-level AND/EXOR expressions. Experiments have shown that the belief that AND/EXOR circuits in general have good testability properties is wrong. The experiments point out that in many cases ESOP circuits are even worse testable than SOP circuits.

Only by modification of the circuit structure (e.g. by using extra test inputs) testability can be improved [12, 19].

References

[1] D. Brand and T. Sasao. Minimization of AND-EXOR expressions using rewrite rules. *IEEE Trans. on Comp.*, 42:568–576, 1993.

[2] R.K. Brayton, G.D. Hachtel, C. McMullen, and A.L. Sangiovanni-Vincentelli. *Logic Minimization Algorithms for VLSI Synthesis*. Kluwer Academic Publishers, 1984.

[3] M.A. Breuer and A.D. Friedman. *Diagnosis & reliable design of digital systems*. Computer Science Press, 1976.

[4] M. Davio, J.P. Deschamps, and A. Thayse. *Discrete and Switching Functions*. McGraw-Hill, 1978.

[5] R. Drechsler, B. Becker, and N. Göckel. A genetic algorithm for 2-level AND/EXOR minimization. In *SASIMI*, pages 49–56, 1995.

[6] R. Drechsler, M. Theobald, and B. Becker. Fast OFDD based minimization of Fixed Polarity Reed-Muller expressions. In *European Design Automation Conf.*, pages 2–7, 1994.

[7] R.D. Eldred. Test routines based on symbolic logical statements. *Journal of the ACM*, 6(1):33–36, 1959.

[8] M. Escobar and F. Somenzi. Synthesis of AND-EXOR expressions via satisfyability. *IFIP WG 10.5 Workshop on Applications of the Reed-Muller Expansion in Circuit Design*, pages 80–87, 1995.

[9] J. Hartmann. *Analyse und Verbesserung der probabilistischen Testbarkeit kombinatorischer Schaltungen*. PhD thesis, Universität des Saarlandes, 1992.

[10] T. Hirayama and Y. Nishitani. A simplification algorithm of AND/EXOR expressions for multiple-output functions. *IFIP WG 10.5 Workshop on Applications of the Reed-Muller Expansion in Circuit Design*, pages 88–93, 1995.

[11] T. Kozlowski, E. L. Dagless, and J. M. Saul. An enhanced algorithm for the minimization of exclusive-or sum-of-products for incompletely specified functions. In *Int'l Conf. on Comp. Design*, pages 244–249, 1995.

[12] S.M. Reddy. Easily testable realizations for logic functions. In *IEEE Trans. on Comp.*, volume 21, pages 1183–1188, 1972.

[13] I.S. Reed. A class of multiple-error-correcting codes and their decoding scheme. *IRE Trans. on Inf. Theory*, 3:6–12, 1954.

[14] K.K. Saluja and S.M. Reddy. Fault detection test sets for Reed-Muller canonical networks. In *IEEE Trans. on Comp.*, volume 24, pages 995–998, 1975.

[15] A. Sarabi and M.A. Perkowski. Fast exact and quasi-minimal minimization of highly testable fixed-polarity AND/XOR canonical networks. In *Design Automation Conf.*, pages 30–35, 1992.

[16] A. Sarabi and M.A. Perkowski. Design for testability properties of AND/XOR networks. *IFIP WG 10.5 Workshop on Applications of the Reed-Muller Expansion in Circuit Design, Hamburg*, pages 147–153, 1993.

[17] T. Sasao. AND-EXOR expressions and their optimization. In T. Sasao, editor, *Logic Synthesis and Optimization*. Kluwer Academic Publisher, 1993.

[18] T. Sasao. *Logic Synthesis and Optimization*. Kluwer Academic Publisher, 1993.

[19] T. Sasao. Easily testable realizations for generalized Reed-Muller expressions. In *Asian Test Symp.*, pages 157–162, 1994.

[20] T. Sasao. Representation of logic functions using EXOR operators. *IFIP WG 10.5 Workshop on Applications of the Reed-Muller Expansion in Circuit Design*, pages 11–20, 1995.

[21] J. Saul. Logic synthesis for arithmetic circuits using the Reed-Muller representation. In *European Conf. on Design Automation*, pages 109–113, 1992.

[22] N.A. Touba and E.J. McCluskey. Automated logic synthesis of random pattern testable circuits. In *Int'l Test Conf.*, pages 174–183, 1994.