

Publications of Ilia Polian

Erdős-Nummer: 3 (through John Hayes and Frank Harary).

H-Index: 11 (measured using Harzing's Publish or Perish): Publications [J11], [J10], [J9], [J7], [C38], [C22], [C18], [C15], [C8], [C1] and [W19] have 11 or more citations.

H-Index of last 5 years: 10.

Book, Book Chapter

- [B3] B. Becker and I. Polian. Fault modeling for simulation and ATPG. In *H.-J. Wunderlich (editor). Models in Hardware Testing*. Springer, to appear 2009 (publication approved).
- [B2] I. Polian. On Non-standard Fault Models for Logic Digital Circuits: Simulation, Design for Testability, Industrial Applications. In *D. Wagner et al. Ausgezeichnete Informatikdissertationen 2003 (Best Dissertations in Computer Science 2003)*. Lecture Notes in Informatics. Volume D-4. GI. Pages 169-178. 2004. ISBN: 3-88579-408-X.
- [B1] I. Polian. On Non-standard Fault Models for Logic Digital Circuits: Simulation, Design for Testability, Industrial Applications. VDI Fortschritt-Berichte, Reihe 20, Nr. 377. VDI-Verlag, Düsseldorf. 218 p. March 2004. ISBN: 3-18-337720-9.

Journal Articles

- [J15] P. Engelke, B. Becker, M. Renovell, J. Schloeffel, B. Braitling, and I. Polian. SUPERB: Simulator Utilizing Parallel Evaluation of Resistive Bridges. *ACM Trans. on Design Automation of Electronic Systems*. Accepted for publication.
- [J14] P. Engelke, I. Polian, M. Renovell, S. Kundu, B. Seshadri, and B. Becker. On detection of resistive bridging defects by low-temperature and low-voltage testing. *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*. 27(2), 2008. Pages 327–338. (ISSN: 0278-0070)
- [J13] I. Polian and H. Fujiwara. Functional constraints vs. test compression in scan-based delay testing *Jour. of Electronic Testing: Theory and Applications*. 23(5), 2007. Pages 445–455. (ISSN: 0923-8174)
- [J12] I. Polian, A. Czutro, S. Kundu, and B. Becker. Power droop testing. *IEEE Design & Test Magazine*. 24(2), 2007. Pages 276–284 (ISSN: 0740-7475)
- [J11] P. Engelke, I. Polian, M. Renovell, and B. Becker. Simulating resistive bridging and stuck-at faults. *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 25(10), 2006. Pages 2181–2192 (ISSN: 0278-0070)
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- [J9] P. Engelke, I. Polian, M. Renovell, and B. Becker. Automatic test pattern generation for resistive bridging faults. *Jour. of Electronic Testing: Theory and Applications*, 22(1), 2006. Pages 61–69. (ISSN: 0923-8174)
- [J8] B. Becker, S. Hellebrand, I. Polian, B. Straube, and H.-J. Wunderlich. DFG project RealTest – test and reliability of nano-electronic systems (in German). *it-Information Technology*. 48(5), 2006. Pages 304–311. (ISSN: 1611-2776)
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- [J6] I. Polian. Nichtstandardfehlermodelle für digitale Logikschaltkreise: Simulation, prüfgerechter Entwurf, industrielle Anwendungen. *it-Information Technology*. 47(3), 2005. Pages 172–174 (ISSN: 1611-2776; abstract of the Ph.D. thesis; selected for publication as one of the candidates for the German Informatics Society Dissertation Award 2003)

- [J5] I. Polian, I. Pomeranz, S. Reddy and B. Becker. On the use of maximally dominating faults in n -detection test generation. *IEE Proceedings Computers and Digital Techniques*, 151(3), 2004. Pages 235–244. (ISSN: 1350-2387)
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- [J3] J. Bradford, H. DeLong, I. Polian, and B. Becker. Simulating realistic bridging and crosstalk faults in an industrial setting. *Jour. of Electronic Testing: Theory and Applications*, 19(4), 2003. Pages 387–395. (ISSN: 0923-8174)
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- [J1] I. Polian and B. Becker. Multiple scan chain design for two-pattern testing. *Jour. of Electronic Testing: Theory and Applications*, 19(1), 2003. Pages 27–48. (ISSN: 0923-8174)

Papers in Formal Proceedings (Refereed)

- [C59] M. Hunger, S. Hellebrand, A. Czutro, I. Polian, and B. Becker. ATPG-based grading of strong fault-secureness. Proc. *IEEE Int'l On-Line Test Symp.*, Lisbon, PT, 2009. (In press)
- [C58] N. Houarche, M. Comte, M. Renovell, A. Czutro, P. Engelke, I. Polian, and B. Becker. An electrical model for the fault simulation of small delay faults caused by crosstalk-aggravated resistive short defects. Proc. *IEEE VLSI Test Symp.*, Santa Cruz, CA, USA, 2008. (In press)
- [C57] K.P. Ganeshpure, I. Polian, S. Kundu, and B. Becker. Reducing temperature variability by routing heat pipes. Proc. *IEEE Great Lakes Symp. on VLSI*, Boston, MA, USA, 2009. (In press)
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- [C55] V. Izosimov, I. Polian, P. Pop, P. Eles, and Z. Peng. Analysis and optimization of fault-tolerant embedded systems with hardened processors. Proc. *Design, Automation and Test in Europe*, Nice, F, 2009. (In press)
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- [C52] I. Polian and W. Rao. Selective hardening of NanoPLA circuits. Proc. *IEEE Int'l Symp. on Defect and Fault Tolerance*, Cambridge, MA, USA, 2008. (In press)
- [C51] I. Polian, S.M. Reddy, I. Pomeranz, X. Tang, and B. Becker. On reducing circuit malfunctions caused by soft errors. Proc. *IEEE Int'l Symp. on Defect and Fault Tolerance*, Cambridge, MA, USA, 2008. (In press)
- [C50] S. Hillebrecht, I. Polian, P. Engelke, B. Becker, M. Keim, and W.-T. Cheng. Extraction, simulation and test generation for interconnect open defects based on enhanced aggressor-victim model. Proc. *IEEE Int'l Test Conf.*, Santa Clara, CA, USA, 2008. (In press)
- [C49] D. Nowroth, I. Polian, and B. Becker. A study of cognitive resilience in a JPEG compressor. Proc. *IEEE/IFIP Int'l Conf. on Dependable Systems and Networks – Dependable Computing and Communications Symp.*, pages 32–41, Anchorage, AK, USA, 2008 (ISBN: 978-1-4244-2398-9).

- [C48] I. Polian, S. Reddy, and B. Becker. Scalable calculation of logical masking effects for selective hardening against soft errors. Proc. *IEEE Int'l Symp. on VLSI*, pages 257–262, Montpellier, F, 2008. (ISBN: 978-0-7695-3179-0)
- [C47] I. Polian, Y. Nakamura, P. Engelke, S. Spinner, K. Miyase, S. Kajihara, B. Becker, and X. Wen. Diagnosis of realistic defects based on the X-Fault model. Formal proc. *IEEE Int'l Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS)*, pages 263–266, Bratislava, SK, 2008. (ISBN: 978-1-4244-2276-0; poster)
- [C46] A. Czutro, N. Houarche, P. Engelke, I. Polian, M. Comte, M. Renovell, and B. Becker. A simulator of small-delay faults caused by resistive-open defects. Proc. *IEEE European Test Symp.*, pages 113–118, Verbania, I, 2008. (ISBN: 978-0-7695-3150-2)
- [C45] C.G. Zoellin, H.-J. Wunderlich, I. Polian, and B. Becker. Selective hardening in early design steps. Proc. *IEEE European Test Symp.*, pages 185–190, Verbania, I, 2008. (ISBN: 978-0-7695-3150-2)
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- [C39] I. Polian, D. Nowroth, and B. Becker. Identification of critical errors in imaging applications. Proc. *IEEE Int'l On-Line Test Symp.*, pages 201–202, Heraklion, GR, 2007. (ISBN: 0-7695-2918-6; poster)
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- [C35] M. Renovell, M. Comte, I. Polian, P. Engelke, and B. Becker. Analyzing the memory effect of resistive open in CMOS random logic. Proc. *Int'l Conf. on Design and Test of Integrated Systems in Nanoscale Technology*, pages 251–256, Tunis, TN, 2006. (ISBN: 0-7803-9726-6)
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- [C30] S. Spinner, M. Doelle, P. Ruther, I. Polian, O. Paul, and B. Becker. A system for electro-mechanical reliability testing of MEMS devices. Proc. *ASM International Symp. for Testing and Failure Analysis*, pages 147–152, Austin, TX, USA, 2006. (ISBN: 0-87170-844-2)
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- [C21] I. Polian, S. Kundu, J.M. Galliere, P. Engelke, M. Renovell, and B. Becker. Resistive bridge fault model evolution from conventional to ultra deep submicron technologies. Proc. *IEEE VLSI Test Symp.*, pages 343–348, Palm Springs, CA, USA, 2005. (ISBN: 0-7695-2314-5)
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Workshop Contributions (Refereed)

- [W30] K.P. Ganeshpure, I. Polian, S. Kundu, and B. Becker. Reducing temperature variability by routing heat pipes. In *DATE Workshop on Process Variability*, Nice, FR, 2009 (Poster).
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- [W6] I. Polian, W. Günther, and B. Becker. The case for 2-POF. In *ITG/GI/GMM-Workshop "Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen"*, Bremen, D, 2003.
- [W5] I. Polian, and B. Becker. Optimal bandwidth allocation in concurrent SoC test under pin number constraints. In *IEEE Workshop on RTL ATPG and DfT*, Guam, USA, 2002.
- [W4] I. Polian, I. Pomeranz, and B. Becker. Exact computation of maximally dominating faults and its application to n -detection tests. In *IEEE European Test Workshop*, Korfu, GR, 2002. (poster)
- [W3] J. Bradford, H. Delong, I. Polian, and B. Becker. Realistic fault simulation in an industrial setting. In *GI/ITG Workshop "Testmethoden und Zuverlässigkeit von Schaltungen und Systemen"*, Bad Herrenalb, D, 2002.
- [W2] I. Polian and B. Becker. Multiple scan chain design for two-pattern testing. In *IEEE Latin American Test Workshop*, pages 156–161, Cancun, MX, 2001.
- [W1] I. Polian, W. Günther, and B. Becker. Efficient pattern-based verification of connections to intellectual property cores. In *ITG/GI/GMM-Workshop "Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen"*, pages I:111–120, Meissen, D, 2001.

Tutorial, Panel (Refereed)

- [T5] "Test of power supply noise – causes, effects and testing." Tutorial presenter. *Int'l Workshop on Impact of Low-Power design on Test and Reliability*, Sevilla, E, 2009.
- [T4] "Benchmarking academic DFT tools on the OpenSparc microprocessor." Panelist. *Int'l Test Conf.*, Santa Clara, CA, USA, 2008.
- [T3] "Defect-tolerance, error-tolerance: which way to go? How?" Panelist. *IEEE Workshop on RTL ATPG and DfT*, Beijing, CN, 2007.
- [T2] "Error-tolerance: are good-enough chips good-enough?" Panel organization and moderation. *IEEE European Test Symp.*, Freiburg, D, 2007.
- [T1] "Soft errors in micro and nanoelectronics." Embedded tutorial. *GMM/GI/ITG Reliability and Design Conf.*, Munich, D, 2007.

Invited Presentations (Not refereed)

1. "Test and reliability of nanoscale electronic systems: next-generation solutions for next-generation challenges". University of Southern California, Los Angeles, USA, October 2008 (Host: Prof. Dr. Sandeep Gupta).
2. "Test, verification and validation of products". Endress & Hauser Flowtec, Reinach, Switzerland, May 2007 (Host: Dr. Ulrich Kaiser).

3. “Resource-constrained error handling in digital circuits”. Intel Santa Clara, USA, May 2007 (Host: Dr. Abhijit Jas).
4. “Transient-error tolerance”. South European Test Seminar, Sestriere, Italy, March 2006.
5. “Transient-error tolerance”. Nara Institute of Science and Technology (NAIST), Nara, Japan, November 2006 (Host: Prof. Hideo Fujiwara).
6. “Transient-error tolerance”. Yale University, New Haven, USA, October 2006 (Host: Prof. Yiorgos Makris).
7. “Power droop in high-performance ICs and a screening strategy”. AMD Boston Design Center, Acton, USA, October 2006 (Host: Dr. Thomas Clouqueur).
8. “Power droop in high-performance ICs and a screening strategy”. University of Massachusetts, Amherst, USA, September 2006 (Host: Prof. Sandip Kundu).
9. “Period of grace: a new paradigm for efficient soft error hardening”. South European Test Seminar, Neustift im Stubaital, Austria, March 2006.
10. “Period of grace: a new paradigm for efficient soft error hardening”. Freiburg-Innsbruck-Paderborn-Stuttgart Workshop, Freudenstadt, November 2005.
11. “Test & diagnosis in nanoscale technologies”. Tokyo Metropolitan University, Tokyo, Japan, October 2005 (Host: Prof. Kazuhiko Iwasaki).
12. “Test & diagnosis in nanoscale technologies”. Osaka Gakuin University, Osaka, Japan, September 2005 (Host: Prof. Kozo Kinoshita).
13. “Soft errors: the fourth dimension”. Nara Institute of Science and Technology (NAIST), Nara, Japan, September 2005 (Host: Prof. Hideo Fujiwara).
14. “Test & diagnosis in nanoscale technologies”. Kyushu Institute of Technology, Fukuoka, Japan, September 2005 (Host: Prof. Seiji Kajihara).
15. “Test & diagnosis in nanoscale technologies”. Nara Institute of Science and Technology (NAIST), Nara, Japan, August 2005 (Host: Prof. Hideo Fujiwara).
16. “Test & diagnosis in nanoscale technologies”. Annual Meeting of the Professorial Advisory Board of the German Informatics Society (GIBU), Dagstuhl, Germany, March 2005 (four of the finalists of the GI Best Dissertations 2003 Award were invited).
17. “Non-concurrent BIST for soft error detection”. South European Test Seminar, St. Leonhard, Austria, March 2005.
18. “Transient fault modeling and detection in dynamic noisy environments”. Freiburg-Innsbruck-Stuttgart Workshop, Innsbruck, Austria, December 2004.
19. “The pros and cons of Very-Low-Voltage testing”. University of Michigan, Ann Arbor, USA, October 2004 (Host: Prof. John P. Hayes).
20. “The pros and cons of Very-Low-Voltage testing”. Stanford University, USA, April 2004 (Host: Prof. Edward McCluskey).
21. “Maximally dominating faults and n -detection”. Freiburg-Innsbruck-Stuttgart Workshop, Freiburg, November 2003.
22. “System-on-a-chip test: an overview and a new result”. Princeton University, USA, December 2002 (Host: Prof. Niraj Jha).
23. “System-on-a-chip test: an overview and a new result”. University of Wisconsin, Madison, USA, December 2002 (Host: Prof. Kewal Saluja).
24. “Maximally dominating faults and n -detection”. Purdue University, West Lafayette, USA, November 2002 (Host: Prof. Irith Pomeranz).
25. “Defect-based test”. Micronas GmbH, Freiburg, Germany, November 2001 (Host: Hartmut Delong).
26. “BIST for delay faults”. University of Iowa, Iowa City, USA, August 1999 (Host: Prof. Sudhakar Reddy).