South European Test Seminar

2008

(SETS'08)

Technical Program

University Center Obergurgl
Tirol, Austria

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Program overview

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Technical Program

Wednesday, March 19

Session 1: DFT & BIST
Moderator: C. Landrault (LIRMM)

1. Optimized Scan Chain Configurations for Diagnosis and Low Power – M. Elm (Stuttgart)
2. Scan Chain Implementation with the Standard Tools (short) – N. Yakymets (Stuttgart)
3. Fault Tolerant Latches, Flip-Flops and Registers – M. Imhof (Stuttgart)

Session 2: ATPG
Moderator: S. Pravossoudovitch (LIRMM)

1. Verification and Analysis of Self-Checking Properties through ATPG – M. Hunger (Paderborn)
2. Automatic Test Pattern Generation for Interconnect Open Defects – S. Spinner (Freiburg)

Session 3: Diagnosis
Moderator: I. Polian (Freiburg)

1. Locating Bugs and Distortions in the Silicon Desert – S. Holst (Stuttgart)
2. Case Study on Logic Diagnosis – Y. Benabboud (LIRMM)
3. An Enhanced Protocol for NoC Test and Diagnosis – R. Ibers (Paderborn)

Thursday, March 20

Session 4: Novel design and test techniques
Moderator: S. Hellebrand (Paderborn)

1. Defect and fault tolerance for crossbar based nanoelectronic PLAs – W. Rao (Chicago)
2. Wireless Test – Z. Noun (LIRMM)
3. Comparison of Asynchronous Design Styles Based on a Network-on-a-Chip Switch (short) – M. Kaufmann (Stuttgart)

Session 5: Bridge defects

Moderator: H.-J. Wunderlich (Stuttgart)
1. Modeling for weak-bridge defect in presence of crosstalk – N. Houarche (LIRMM)
2. Resistive Bridging Fault Simulation of Industrial Circuits – P. Engelke (Freiburg)

Session 6: BIST
Moderator: G. Di-Natale (LIRMM)

1. Programmable Deterministic Self-Test – A. Hakmi (Stuttgart)
2. Signature Rollback - A Technique for Testing Robust Circuits – U. Amgalan (Paderborn)
3. Pseudo-Exhaustive Test Patterns Generation for Large Circuits (short) – A. Mumtaz (Stuttgart)

Friday, March 21

Session 7: Memory test
Moderator: H.-J. Wunderlich (Stuttgart)

1. A History-based Diagnosis Technique for Static and Dynamic Faults in Memories (double talk) – A. Bosio / L. Dilillo (LIRMM)
2. A Modular Memory BIST for Optimized Memory Repair – P. Oehler (Paderborn)

Session 8: Fault modeling
Moderator: M. Comte (LIRMM)

1. A Simulator of Small-Delay Faults Caused by Resistive-Open Defects – A. Czutro (Freiburg)
2. Single-Event Transient Masking: Impact on modeling and mitigation – C. Zoellin (Stuttgart)

Session 9: Yield and reliability
Moderator: W. Rao (Chicago)

1. Yield improvement, fault-tolerance to the rescue? – J. Vial (LIRMM)
2. Reliability Model for Hardware-Software Systems – M. Kochte (Stuttgart)
3. Reliability Modeling - Model Evaluation – R. Baranowski (Stuttgart) – short

Abstracts

Session 1: DFT & BIST

Moderator: C. Landrault (LIRMM)

Optimized Scan Chain Configurations for Diagnosis and Low Power

Melanie Elm, University of Stuttgart

Scan design, where hundreds or thousands of scan-chains are employed, saves an enormous amount of time during test and thus is a strong necessity for recent industrial designs.

Despite the facilitations and performance enhancements multiple scan chains entail, this methodology introduces new problems. Using multiple scan-chains, the question arises, which scan-flip-flops should be grouped together to form one chain. To solve this adequately several application specific issues have to be taken into account. One of theses issues is the fault-aliasing and fault cancellation which occurs with any of the recent compaction techniques for test responses. Another issue is the power consumption during test application, as the scan cell organization has influence on the switching activity on the one hand and the effectiveness of test planning strategies for low power on the other hand.

In this talk a methodology and an algorithm for optimal scan chain clustering is proposed. Two applications are analyzed, first the maximization of diagnostic resolution under the employment of different space compactors and second the optimization of power consumption by disabling scan chains.

In both cases the results show a significant improvement compared to layout driven scan chain clustering. The method perfectly fits into a standard tool flow and leaves sufficient degrees of freedom to the tools to optimize the routing overhead.

Scan Chain Implementation with the Standard Tools (short)

Natalia Yakymets, University of Stuttgart

Scan insertion is critical to many other DFT techniques, but it is a tedious task to perform manually. Decisions during Scan chain insertion can have large impact on design routability, wire length, area, timing and power. Furthermore, it is a lot of extensive research that proposes scan chain organization for certain targets including reordering for area and power minimization, clustering for fault diagnosis, etc. Nevertheless, almost all of them consider design at the high level and do not address the issue of impact of high level constraints to a real layout. Scan chain reordering based on physical design information helps in reducing routing overhead and in minimizing design constraint violations.

The current work tends to research how the real layout is influenced by high level constraints. It presents the most common scan insertion approaches. These approaches and the associated parameters such as clustering strategy and length of the scan chains are than evaluated with respect to the wire length and area overhead after place and route. For the comparison, two commercial tools have been used to implement scan chain insertion for the ISCAS and ITC circuits. The results obtained clearly indicate the advantages and drawbacks of each reordering technique under consideration.

Session 1: DFT & BIST (cont'd)

Fault Tolerant Latches, Flip-Flops and Registers
Michael Imhof, University of Stuttgart

Due to the system integration on chip the amount of integrated memories like latches, flip-flops and registers is increasing compared to random logic.
The linear dependency between area and sensitivity against particle strikes influences the vulnerability of on chip memories in two ways. First the fraction of die area used for memory is increasing and thereby the amount of errors introduced in storage elements. Second the shrinking structure sizes lead to a reduced critical charge needed to change the stored value. This further increases the soft error rate.
On chip memories can be considered a major source for Single Event Upsets (SEUs).
The design optimization for low power amplifies this effect as many functional units are not actively used most of the time. These long periods of data retention lead to fault accumulation.

Existing approaches for highly reliable storage elements are expensive in terms of either die area or wiring. As the design paradigms are shifting from single cores to complex systems with multiple cores on a single die the customers are not satisfied with reduced system reliability and are even requesting a continued increase in reliability.
In this talk, a method to protect integrated memories like flip-flops and latches based on error detection and correction is presented. The properties of the developed scheme include:

- Regular structure: Aggregation into few standard cell types which can be reused
- Fully integrated into the existing scan chain
- Same fault detection rate compared to other approaches
- Possibility of fault correction: Identification of the faulty cell
- Low hardware-overhead
- Cheap wiring in high metal layers above the scan chain.

Session 2: ATPG

Moderator: S. Pravossoudovitch (LIRMM)

Verification and Analysis of Self-Checking Properties through ATPG

Marc Hunger, University of Paderborn

Present and future semiconductor technologies are characterized by increasing parameters variations as well as an increasing susceptibility to external disturbances. Transient errors during system operation are no longer restricted to memories but also affect random logic, and a robust design becomes mandatory to ensure a reliable system operation. Self-checking circuits rely on redundancy to detect and compensate errors online. However, during synthesis and optimization self-checking properties can be destroyed. This paper shows how automatic test pattern generation (ATPG) can be used to analyze self-checking properties. As a result the properties are either verified or the fault detection profile provided by ATPG can be used to increase the error detection or fault tolerance capabilities of the design. Experimental data are shown for several self-checking arithmetic circuits.

Automatic Test Pattern Generation for Interconnect Open Defects

Stefan Spinner, Albert-Ludwigs-University of Freiburg

We present a fully automated flow to generate test patterns for interconnect open defects. Both inter-layer opens (open-via defects) and arbitrary intra-layer opens can be targeted. An aggressor-victim model used in industry is employed to describe the electrical behavior of the open defect. The flow is implemented using standard commercial tools for parameter extraction (PEX) and test generation (ATPG). A highly optimized branch-and bound algorithm to determine the values to be assigned to the aggressor lines is used to reduce both the ATPG efforts and the number of aborts. The resulting test sets are smaller and achieve a higher defect coverage than stuck-at *n*-detection test sets, and are robust against process variations.

Session 3: Diagnosis

Moderator: I. Polian (Albert-Ludwigs-University of Freiburg)

Locating Bugs and Distortions in the Silicon Desert
Stefan Holst, University of Stuttgart

In modern chip production, volume diagnosis is essential to increase yield. Rising design complexity and process variations does not allow for simulating silicon behavior or limiting to fault models.

Due to time and memory constraints during high volume test, the failure information available for diagnosis is already very limited today. Our generalization of the SLAT approach considers all available failure information to point out suspect circuit regions.

In current multi site testing and self diagnosis environments it is not only crucial to use as much information as possible to gain the optimal diagnostic resolution. The test response data volume becomes the most critical factor for the test cost and is usually highly compacted.

What are the implications of such environments on logic diagnosis? How can logic diagnosis cope with highly compacted response data? What influence have the compaction methods on diagnostic resolution? How much response data is necessary to achieve the best resolution?

This talk gives some answers to these and other questions.

Case Study on Logic Diagnosis
Youssef Benabboud, LIRMM

In this paper we present a case study on logic diagnosis based on the effect-cause methodology implemented in the DERRIC tool.

We therefore evaluate DERRIC on an industrial circuits of STMicroelectronics.

First of all we modify the DERRIC flow in order to take in account the problems related to the industrial circuits. Finally, we compare DERRIC (Lirmm tool) results with Tetramax (Synopsys tool) results and YieldTracker (ST tool) results.

An Enhanced Protocol for NoC Test and Diagnosis
Ruediger Ibers, University of Paderborn

The use of embedded systems in our daily life constantly grows, whereby reliability and a long life cycle of such systems are demanded. Network on Chips (NoC) are considered as the communication architecture for future System on Chip (SoC) designs. To cope with failures due to degradation or external disturbances during the life time of a system, diagnostic capabilities are required to
exploit the inherent redundancies in NoCs. Thus, the NoC prototype developed in Paderborn has been extended to support the detection and the diagnosis of permanent and temporary errors on interconnections and network nodes. The protocol is enhanced, such that adjacent nodes can test and diagnose each other or the interconnections between them. This way test and diagnosis possibilities can be provided with only a small hardware overhead. The proposed protocol is verified by a network simulator. Furthermore a diagnosis controller is under development to keep the diagnosis process more flexible and to reduce the network traffic overhead.

Session 4: Novel design and test techniques
Moderator: S. Hellebrand (University of Paderborn)

Defect and fault tolerance for crossbar based nanoelectronic PLAs
Wenjing Rao, University of Illinois at Chicago

Programmable logic arrays (PLAs) are promising as platforms for nanoelectronic logic, since they are highly regular and can be supported by the nano crossbar architectures. Reliability is a severe challenge as far as nanoelectronic devices are concerned. It is therefore necessary to focus on the defect and fault tolerance aspects of nanoelectronic PLAs to ensure their viability as a foundation for nanoelectronic systems. This talk includes a discussion on the main challenges and various opportunities of developing reliable nanoelectronic PLAs. Specifically, the massive defects in the fabric impose strict constraints to the function mapping process. Therefore, the process of function mapping, which used to be a trivial phase in the logic design process, emerges as a new challenge. For online fault tolerance, the challenges and explorations of fault masking and online repair strategies will be presented.

Wireless Test
Ziad Noun, LIRMM

Testing is not used only to find the fault free devices and systems in order to insure a high quality production, but also to improve production yield at various stages of manufacturing by analyzing the cause of defects when faults are encountered. However, the actual test is performed by contact, which is an efficient solution, but it suffers from two main disadvantages:
1) Limited number of dies tested simultaneously, which means a large time to test an entire wafer.
2) Substrate scrubbing pads due to multi contacts, which limits the number of recursive test (critical for System in Package test)

My work aims to integrate a radio interface (antenna and Transceiver) in each IC, in order to establish a wireless link (without contact) between ICs and tester. The resulted wafer will resemble to a network of wireless nodes served by the tester, which is equipped by a radio interface, on its turn.
The wireless test could be used also to perform an in-situ test (test of the device during its normal life), device reprogramming and others.

A general overview of the wireless test and its possible applications, with an investigation of the power supply during wireless wafer test will be the subjects of my presentation.

Session 4: Novel design and test techniques (cont'd)

Comparison of Asynchronous Design Styles Based on a Network-on-a-Chip Switch (short)
Michael Kaufmann (University of Stuttgart)

For several years asynchronous design styles gained a lot of attention in academic research and industry. Several asynchronous chips have been designed and produced resulting in new concepts. One of these concepts is Globally Asynchronous Locally Synchronous (GALS) which combines the properties of asynchronous and synchronous concepts: The global communication of the chip is implemented asynchronously whereas the IP cores are still clocked.

This study thesis compares the two most important asynchronous design styles: The self-timed and the quasi-delay insensitive asynchronous design styles are examined based on the implementation of an asynchronous Network-on-a-Chip switch. Properties of asynchronous designs in general and both examined design styles are presented. Furthermore development effort, area usage, performance and robustness against parameter variations get compared. Finally, a comprehensive overview of the implementation process of asynchronous circuits in VHDL is given. This also emphasizes some of the most important differences between synchronous and asynchronous circuit development.

A currently nearly unexplored area is the test of asynchronous circuits which prevents widespread usage. This includes but is not limited to the questions on how to implement Built In Self Test (BIST) in asynchronous circuits as well as the on chip generation of test patterns. These questions will be explored in a diploma thesis and verified using the implemented asynchronous NoC switch.

Session 5: Bridge defects

Moderator: H.-J. Wunderlich (University of Stuttgart)

Modeling for weak-bridge defect in presence of crosstalk

Nicolas Houarche, LIRMM

This paper proposes a behavioural analyse of a resistive weak-bridge as a function of its unpredictable resistance R_b. Considering the short-cut is aggravated by crosstalk represented with a coupling capacitance C_m, some other parameters, such as the skew, have to be considered.
Finally, a model is proposed to determine the defect resistance interval, by knowing the skew and the slack time of the path.

Resistive Bridging Fault Simulation of Industrial Circuits

Piet Engelke, Albert-Ludwigs-University of Freiburg

We report the successful application of a resistive bridging fault (RBF) simulator to industrial benchmark circuits. Despite the slowdown due to the consideration of the sophisticated RBF model, the run times of the simulator were within an order of magnitude of the run times for pattern-parallel complete-circuit stuck-at fault simulation. Industrial-size circuits, including a multi-million-gates design, could be simulated in reasonable time despite a significantly higher number of faults to be simulated compared with stuck-at fault simulation.

Session 6: BIST
Moderator: G. Di-Natale (LIRMM)

Programmable Deterministic Self-Test
Abdulwahid Hakmi, University of Stuttgart

The standard self-test approaches are a variation of mixed-mode self-test schemes known as reseeding and test set embedding. In these schemes easy faults are detected by random patterns while the hard faults are targeted by deterministic patterns. The random patterns are generated cost effectively by running a pseudo random pattern generator like Linear Feedback Shift Register (LFSR) in autonomous mode while for deterministic patterns one of the two approaches is adopted.

In reseeding, deterministic patterns are encoded as the seeds of an LFSR which are stored in memory. It has been shown analytically that reseeding is optimal with respect to entropy and the available reseeding approaches already reach the maximum encoding efficiency that could be achieved using this approach. The main advantage of reseeding is that it is programmable while the disadvantage includes the requirement of significant storage. In test set embedding, deterministic patterns are embedded into pseudorandom sequence by changing some bits in useless patterns. This is done with the help of an on-chip combinational logic called bit flipping or bit fixing logic. The main advantage of this approach is less information storage compared to reseeding while the disadvantage is that the test information is stored hardwired which makes it test set dependent.

Although both approaches offer a good reduction in test data volume but low cost test for rapidly growing circuits necessitates the development of new test methods that could drastically reduce test data volume while maintaining programmability with minimum hardware overhead. In this talk I shall present how this goal can be achieved by exploiting the synergy between efficient but hardwired test set embedding and programmable but less efficient compression techniques in multiple ways.

The first choice is to partition the test circuitry and implement the most expensive part i.e. embedding information off-chip as BOST. But to retain programmability this embedding information is stored in memory and to reduce memory and communication overhead it is stored in compressed form. A special decoder is then implemented on-chip which is totally independent of the test set and has the ability to decode a code in parallel in a single clock. This approach significantly reduces the hardware overhead compared to embedded built-in self-test on the cost of small increase in test time.

The second choice named “Nearly complete reseeding” takes advantage of the LFSR encoding characteristics to implement an efficient programmable BIST scheme. It is based on the observation that significantly more care bits can be encoded in the seed of a LFSR, if a limited number of conflicting equations is ignored in the employed linear equation system. The ignored care bits are separately embedded into the LFSR pattern. In contrast to known deterministic BIST schemes based on test set embedding, the embedding logic function is not hardwired. Instead, this information is stored in memory using a special compression and decompression method. This approach shows significant reduction in storage requirements compared to pure reseeding solutions.

A third approach named “Restrict encoding” uses the fact that a large number of test vectors at similar positions in a pattern set are compatible and could be generated using a single fully specified test vector. The idea is to restrict vectors at such positions to a value that covers care bits of all the vectors at those positions and encode the vectors at unrestricted positions with the seeds. The restrict information is stored in memory along with the seeds and during test the vectors at restricted positions are shifted into scan chains from memory instead of LFSR outputs. This approach achieves similar efficiency like “Nearly complete reseeding” while making the control bit simpler because no decompression is required and the embedding information is stored in memory in ready to use form.

All these three novel methods along with experimental results for benchmark circuits and industrial designs will be presented in this talk.

Session 6: BIST (cont’d)

Signature Rollback - A Technique for Testing Robust Circuits
Uranmanddakh Amgalan, University of Paderborn

Dealing with static and dynamic parameter varia tions has become a major challenge for design and test. To avoid unnecessary yield loss and to ensure reliable system operation a robust design has become mandatory. However, standard structural test proce dures still address classical fault models and cannot deal with the non-deterministic behavior caused by parameter varia tions and other reasons. Chips may be rejected, even if the test reveals only non-critical fail ures that could be com pensated during system operation. This paper introduces a scheme for embedded test, which can distinguish critical permanent and non-critical transient failures for circuits with time redun dancy. To minimize both yield loss and the overall test time, the scheme relies on partitioning the test into shorter ses sions. If a faulty signature is observed at the end of a session, a roll back is triggered, and this par ticular session is repeated. An analyti cal model for the ex pected overall test time pro vides guidelines to deter mine the opti mal para meters of the scheme.

Pseudo-Exhaustive Test Patterns Generation for Large Circuits (short)
Abdullah Mumtaz, University of Stuttgart

Pseudo-Exhaustive Testing is a BIST approach in which a large circuit is partitioned into fanin cones by backtracking from each Primary Output (PO) through the circuit to the Primary Inputs (PI) that influence that output. Each of the partitions is tested exhaustively.

It has the advantage of testing the portion of the circuit (fanin cones) exhaustively with advantages like extremely high fault coverage, the generality of the fault model and ease of generating the test set.

Proposed by McCluskey in 1984, this scheme became impractical as the circuits became larger and Primary Outputs (PO) depending on large number of primary Inputs (PI).

As today’s circuits are getting faster, their depths (critical paths) are reducing as well. Hence we can expect a significant portion of the circuit that can be covered Pseudo- Exhaustively.

In this talk, I will present initial analysis that shows the potential to cover large portion of the industrial circuits Pseudo-Exhaustively. These results indicate the potential of a new scheme to cover this portion of the circuit with few Primitive Polynomials for its Pseudo-Exhaustive testing.

Session 7: Memory test

Moderator: H.-J. Wunderlich (University of Stuttgart)

A History-based Diagnosis Technique for Static and Dynamic Faults in Memories (double talk)

Alberto Bosio (LIRMM)
Luigi Dilillo (LIRMM)

The usual techniques for memory diagnosis are mainly based on signature analysis. They consist in creating a fault dictionary that is used to determine the correspondence between the signature and the fault models affecting the memory. The effectiveness of such diagnosis methods is therefore strictly related to the fault dictionary accuracy. To the best of our knowledge, most of existing signature-based diagnosis approaches targets static faults only. In this paper, we present a new diagnosis approach that represents an alternative to signature-based approaches. This new diagnosis technique, denoted as history-based diagnosis, makes use of the effect-cause paradigm already developed for logic design diagnosis. It consists in creating a database containing the history of operations (read and write) performed on a faulty memory core-cell. This information is crucial to track the root cause of the observed faulty behavior and it can be used to generate the set of possible Fault Primitives, which represents the set of suspected fault models. This new diagnosis method is able to identify static as well as dynamic faults. Although in this paper it is applied to SRAMs, it can be effective also for other memory types. Experimental results are provided to prove the efficiency of the proposed methodology in generating a list of candidate faults as well as the location of faulty components in the memory.

A Modular Memory BIST for Optimized Memory Repair

Philipp Oehler, University of Paderborn

An efficient on-chip infrastructure for memory test and repair is crucial to enhance yield and availability of SoCs. Most built-in self-repair solutions contain IP-Cores for BIST. This gives the advantage of reusing the BIST hardware without modifications, but also prevents an optimized test and repair interaction. In this paper, the concept of modular BIST for memories is introduced. The modularity of the test is achieved with small modifications in the BIST controller. Using the modular test controller, an optimized interaction of test and repair is illustrated using recently proposed repair scheme.

Session 8: Fault modeling
Moderator: M. Comte (LIRMM)

A Simulator of Small-Delay Faults Caused by Resistive-Open Defects
Alejandro Czutro, Albert-Ludwigs-University of Freiburg

We present a simulator which determines the coverage of small-delay faults, i.e. delay faults with a size below one clock cycle, caused by resistive-open defects. These defects are likely to escape detection by stuck-at or transition fault patterns. For the first time, we couple the calculation of the critical size of a small-delay fault with the computation of the resistance range of the corresponding resistive-open defect for which this size is exceeded. By doing so, we are able to extend probabilistic fault coverage metrics initially developed for static resistive bridging faults to small-delay defects.

Single-Event Transient Masking: Impact on modeling and mitigation
Christian Zoellin, University of Stuttgart

Decreasing feature sizes have led to increased vulnerability of random logic to soft errors. In combinational logic a particle strike may lead to a glitch at the output of a gate, also referred to as single even transient (SET), which in turn can propagate to a register and cause a single event upset (SEU) there.
Several factors may prohibit a SET from causing a SEU: Electrical masking, Latch-Window masking, Static and Dynamic Logic masking. This talk provides a detailed discussion of the important effects and tries to estimate the contribution of each effect.
With these effects in mind, the talk will give a short overview of a recent electrical level model for particle strikes as well as mitigation techniques.

Session 9: Yield and reliability

Moderator: W. Rao (University of Illinois at Chicago)

Yield improvement, fault-tolerance to the rescue?
Julien Vial, LIRMM

With the technology entering the nano dimension, manufacturing processes are less and less reliable. Yield will be in decline. Fault tolerant architectures could be use in the future to increase the yield. The fault tolerant system will be able to tolerate manufacturing defects as well as on-line defects. We analyze the conditions to be fulfilled to adopt fault tolerant mechanisms to cover manufacturing defects and therefore improve the yield. As case study, we apply those conditions to a classical fault tolerant architecture such as the Triple Modular Redundancy (TMR) architecture. Moreover, we provide a test solution for the TMR architecture.

Reliability Model for Hardware-Software Systems
Michael Kochte, University of Stuttgart

Estimating the reliability of hardware-software systems allows to determine the robustness of a system and its design alternatives during design exploration. A system model used to derive such a reliability estimate has to incorporate the hardware structure and architecture of the system as well as the performed function. Considering merely the functional model or the structural model separate from the other one may yield an invalid reliability estimation, being either too optimistic or too conservative.
While an architectural model allows to determine the impact of logical and architectural fault masking on the design's error rate, it fails to correctly predict the failure rate of the overall system. The function that is performed by the design exhibits particular usage and communication patterns that may—depending on the function—result in increased or reduced susceptablility to faults.
We propose a model that combines functional aspects with the architecture of the system. Fault injection and simulation show the optimistic resp. pessimistic nature of the simplifying assumptions in models. This results in an invalid reliability estimation w.r.t. a simulation of the integrated system model.

Reliability Modeling - Model Evaluation
Rafal Baranowski, University of Stuttgart

Being a new associate at the ITI Institute, I am engaged in ongoing research on reliability modeling of hardware/software systems in the course of the System Reliability Project (DFG 460). My actual work involves experimental reliability estimation by fault injection and system simulation. To reduce experimental run times, I will explore the subject of circuit instrumentation for efficient hardware fault insertion and system emulation. My future work will address hardware/software partitioning problem for increased system reliability and fault tolerance.