# Selective Hardening in Early Design Steps

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***Abstract*— Hardening a circuit against soft errors should be performed in early design steps before the circuit is laid out. A viable approach to achieve soft error rate (SER) reduction at a reasonable cost is to harden only parts of a circuit. When selecting which locations in the circuit to harden, priority should be given to critical spots for which an error is likely to cause a system malfunction. The criticality of the spots depends on parameters not all available in early design steps. We employ a selection strategy which takes only gate-level information into account and does not use any low-level electrical or timing information.**

**We validate the quality of the solution using an accurate SER estimator based on the new UGC particle strike model. Although only partial information is utilized for hardening, the exact validation shows that the susceptibility of a circuit to soft errors is reduced significantly. The results of the hardening strategy presented are also superior to known purely topological strategies in terms of both hardware overhead and protection.**

***Keywords*— Soft error mitigation, reliability**

## I. Introduction

Hardening parts of the circuit while leaving the other parts unprotected can provide soft error rate (SER) improvement at acceptable cost [1, 2]. Selective hardening can be applied to a circuit's flip-flops [3, 4] as well as combinational logic [5, 6, 7, 8]. Existing methods evaluate the susceptibility of individual gates in a circuit to soft errors which will change the circuit's state and will cause the system to malfunction. The gates with the highest impact are selected for hardening to achieve maximal SER reduction. In a study by NXP [7], the SER could be improved by 60% SER at 20% area overhead. As the local hardening will not make the gate completely immune against particle strike but reduce the susceptibility down to 10 to 20 per cent [7], an economic trade-off between the degree of protection and hardening costs in terms of hardware and design effort is required.

The impact of soft errors at a gate is determined by a number of factors including the probability that a disturbance (e.g., a particle strike) will generate a pulse at the gate output, the probability that a sensitized path exists from the gate to a flip-flop (logical masking), the probability that the pulse arrives at the flip-flop when it accepts new values (latching-window masking), and the probability that the pulse is not attenuated when it propagates through the circuit (electrical masking) [2]. Most of these probabilities can only be accurately determined when technology parameters and layout data not available at the gate level are taken into account. However, selecting gates for hardening after the circuit has been laid out is not practical. The hardening itself would necessitate changes in the layout of the circuit, resulting in a hen-and-egg problem.

In this paper, we investigate an approach to select a minimum number of gates for hardening to reach a reliability target, which only employs static information available at gate level. Then, we validate the quality of the approach using an accurate soft error framework. The framework is based on the novel UGC model optimized for soft errors in nanoscale electronics and takes all masking mechanisms into account [9].

This is the first published paper which validates by accurate soft error simulation that selective hardening done without taking electrical and timing information into account indeed results in an adequate SER improvement. In addition, we compare the results with a selective hardening technique which employs topological information only [10] and show significant gains with respect to hardware overhead and reliability. The remainder of the paper is organized as follows. Previous work is reviewed in Section II. Selective hardening strategies are described in Section III. The technique to validate the found solution is presented in Section IV. Experimental results are reported in Section V. Section VI concludes the paper.

## II. Previous work

A circuit is selectively hardened in two steps: first, a sub-set of its gates with the largest impact on the circuit-level SER is selected, and then a hardening technique is applied to the gates from the selected sub-set. Several approaches to select individual gates for hardening have been proposed in the literature. Mohanram and Touba [5] perform an electrical analysis of the primitive cell library to determine gates susceptible to single-event transients (SETs). The same authors also study coarse-granularity solutions where entire blocks are selected for hardening [1].

Zhao et al. [6] identify soft spots on which signal integrity could deteriorate below an acceptable level due to SETs. Nieuwland et al. [7] determine the SER of each gate using a simplified electrical model and select the gates with the highest

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SER for hardening. A probabilistic analysis is performed in [11] similar to Hayes et al. [8], who estimate the probability $p_{err}$ that an SET which occurs on an internal node of the circuit leads to a visible effect on an output. The nodes are selected for hardening such that $p_{err}$ is minimized below a pre-defined value.

A number of techniques for the second step (actual hardening of the selected gates) are described in the literature. The standard approach relies on sophisticated transistor sizing [12]. Nieuwland et al. [7] propose to duplicate a gate and connect the outputs of both copies of the gate. If the duplicated gate is placed at a sufficient distance to rule out the probability of both gates being affected by the same particle strike, the SER contribution by the hardened gate is reduced by roughly a factor of 8. Garg et al. [10] suggest to supplement the duplication by connecting the outputs of the gates by a diode or a transistor.

## III. Gate-Level Hardening

### A. Problem formulation

Gate-level hardening has to take into account how the susceptibility of a single gate is reduced by local hardening. Multiple techniques have been proposed so far, which differ in the degree of protection and in hardware cost, including [12, 10, 7]. The selective hardening method presented below can take these different techniques into account by using a *local hardening factor* (LHF), which is defined as the factor by which the susceptibility of a gate to soft errors is reduced.

Assume there is a method available for computing the probability $p_{err}$ of an erroneous system output for given susceptibilities of the gates. Complete hardening may not allow us to reduce this below $p_{err}/LHF$. The goal of selective hardening is to find a minimum number of gates and reduce their susceptibility by factor $LHF$ such that the new probability of an erroneous system output is reduced to $c \cdot p_{err}$, where $1/LHF \leq c \leq 1$.

Let $p_f$ be the detection probability of a short pulse on a line $l$. If this pulse fault is a positive glitch, detection requires $l = 0$, dynamically sensitized paths to some flip-flops and the pulse arriving there during the latch window. If $f$ is a negative glitch, $l = 1$ is required. For each fault $f$, $s_f$ is the susceptibility of the corresponding gate to a radiation induced error. $s_f$ depends on both the cell design and the radiation.

The probability of an erroneous output due to fault $f$ is $s_f \cdot p_f$. As this is a rather small number, we can simply sum up:

$$p_{err} = \sum_{f \in C} s_f \cdot p_f \tag{1}$$

This formalization takes into account that a gate can be hardened against positive and negative pulses, and deals with these pulses separately. If we want to reduce the probability of erroneous output by a factor $c$ through hardening against a subset of faults $C_1 \subset C$ with minimum cost, we have to find a minimum set $C_1$ such that

$$c \cdot p_{err} \geq \sum_{f \in C_1} \frac{s_f}{LHF} \cdot p_f + \sum_{f \in C \setminus C_1} s_f \cdot p_f \,. \tag{2}$$

The next subsection describes the required parameters for evaluating (2), which are only available after layout.

### B. Computation model

The computation model is based on several parameters, which complicate the computing procedures on the one hand and are not available before layout on the other hand. These parameters include:

a) *Gate susceptibility* describes the probability and the shape of a glitch produced at a gate's output by a particle strike. This information can be obtained by precise but computationally intensive device simulation [13]. In many cases circuit-level techniques offer a good compromise between accuracy and computational cost [14, 15, 16, 17]. Mixed-level approaches combine device-level analysis for a few devices with circuit-level analysis for the rest of the circuit [18, 13]. Lifting this information up to gate level requires an electrical model of each cell, to be stored in the library. Often, the models introduced in [19, 20, 21] are used. In [9], a refinement of these models called the UGC model is introduced. It shows that the previous models underestimate the error probability significantly, and it will be employed for the experiments in this paper.
Determining the gate susceptibility requires that technology and library are fixed and technology mapping has already been done. It cannot be performed for soft cores, free libraries or in early design steps before technology mapping.

b) *Electrical masking*: CMOS is a self-restoring technology which reshapes signal transitions and filters short pulses. The electrical masking effect depends on both the library cell and the load to be driven. This information is not available before layout.

c) *Latching-windows masking*: The pulse generated by the hit gate must be propagated through the circuit on (multiple) paths and arrive at a latch at a time when the latch is ready to capture data. Latching-window masking blocks all the errors arriving at a different time, and this effect can only be computed after all the wire and switch delays are known. The effect of latching-window masking depends on the travel time of the signal, the operating frequency and the exact clocking scheme. Its precise estimation requires layout information.

d) *Logical masking*: There must be a sensitized path from the hit gate to a latch in order to capture the fault. However, static sensitization of multiple paths successfully employed for stuck-at faults overestimates the masking effect significantly and techniques based on static fault

detection like [8, 11] are inherently imprecise [22]. For instance, if an inverting and a non-inverting path from a pulse location reconverge at an AND gate and both are sensitized, the static analysis will yield logic-0 at the output of the AND gate. However, if the delays of both paths are different, a pulse of the faulty logical value may be generated and propagated to the latches. Static analysis does not catch the propagation of such pulses. Hence, a dynamic analysis has to be performed [23] in a similar way it is done in delay testing or power analysis. Again, the exact timing is required which is not available before layout parameter extraction. If the analysis is performed by an event-driven timing simulator, the dynamic logical masking is automatically accounted for.

### *C. Gate selection*

All the reported techniques for computing the error probability without explicit simulation neglect some or most of the parameters above. Moreover, it does not seem reasonable to spend high effort to obtain exact results with respect to one of the parameters if neglecting the other parameters introduces an even larger effect. For instance, computing static logical masking corresponds to computing stuck-at fault detection probabilities [24], is NP complete and computationally expensive. The results, however, overestimate the logical masking whose computation requires delay fault detection probabilities [25]. For selecting the gates to be hardened, this inaccuracy does not hurt, as we are interested in a relative order of gates with highest impact rather than in absolute values of $p_{err}$.

Equation (2) can be used either to find a minimum set $C_1$ of gates to be hardened, or to find the optimal factor $c$ for reducing the error probability. Assuming all the faults have the identical susceptibility, we do not have to evaluate $s_f$. The $p_f$, however, are pulse detection probabilities, which can be estimated by fault detection probabilities in a coarse way. There exists a plethora of algorithms for estimating stuck-at fault detection probabilities $\tilde{p}_f$, e.g. PROTEST [24], COP [26] or BDD based approaches [27]. Any of them will do, as exact values are not required due to the additional dynamic errors.

The straightforward way also used for the experimental results reported below is dividing the number $|TS(f)|$ of test patterns for the stuck-at faults $f$ by the total number of patterns applied, $\tilde{p}_f = \frac{|TS(F)|}{m}$, for a random test or an exhaustive test with $m = 2^n$, $n$ number of inputs.

A measure for the overall error probability is now

$$\tilde{p}_{err} = \sum_{f \in C} \tilde{p}_f \ , \tag{3}$$

where the $s_f$ are not considered as we are only interested in relative values.

We now select the set $C_1 \subset C$ such that

$$c \cdot \tilde{p}_{err} = \sum_{f \in C_1} \frac{\tilde{p}_f}{LHF} + \sum_{f \in C \setminus C_1} \tilde{p}_f \ . \tag{4}$$

While the absolute numbers of $\tilde{p}_{err}$ are rather meaningless, the experimental data presented below shows that the improvement factor $c$ is well reflected at layout level.

## IV. Validation Technique

While the gate selection takes only static gate-level information into account, the validation is based on the simulation of comprehensive layout information described above. For this purpose, we perform Monte-Carlo simulations using the soft error simulation framework based on the novel UGC model of single-event transients [9]. The framework takes static and dynamic logical, electrical and latching-window masking into account. As it was not the purpose of this work to improve the simulation techniques for SETs at the gate level, a commercial simulator was used for a prototype implementation. To speed up simulation, more advanced techniques can be applied [28].

Furthermore, we apply the soft error simulation framework to study the influence of the local hardening technique on the SER improvement. If several local hardening mechanisms with different efficiency ($LHF$) and costs are available, our data can help to decide whether it is more efficient to select more gates for hardening or to employ the local hardening mechanism with a higher $LHF$.

Figure 1 summarizes the flow of the proposed method. The selective hardening of a circuit (i.e., selection of a given number of errors for hardening) by using only gate-level information is shown above the dashed line. The evaluation of the hardened circuit by taking into account all available electrical information is summarized below. The result of the evaluation is an accurate prediction of the actual SER reduction.

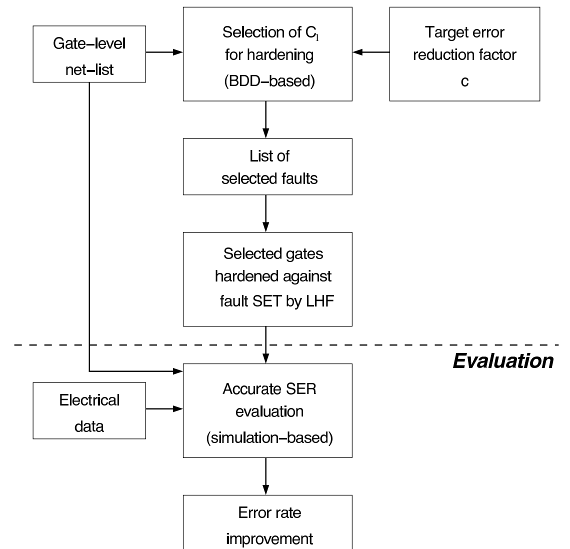


Fig. 1. Flow of gate-level hardening and its validation

## V. Experimental Results

### A. Experimental setup

In contrast to the gate selection method from the previous section which avoided using electrical information, the framework aims at the calculation of numbers which are as accurate as possible. Several methods to estimate SER of a circuit have been proposed in the past [29, 30, 31]. The UGC model targets combinational logic [9] and is applied below.

The framework performs simulation on the gate level using a VHDL simulator. The injection of SETs is performed by looking up the parameters of the pulse resulting from the particle strike in an SET characterization table, which is created ahead of time for a primitive cell library.

*1) SET characterization table:* The SET characterization table is used to derive the characteristics of a pulse induced by a particle strike from the electrical parameters of the particle, the circuit and the affected gate as well as the gates up to $T$ logic levels after the affected gate. The characteristics of the pulse at the output of the gate struck by the particle, in particular its width, depend on the affected $pn$ junction, the logic values applied at the gate's inputs, and the charge injected.

To pre-compute the SET characterization table, the accurate equations have been derived for the UGC model and implemented as a two-terminal network that can be integrated into a VHDL-AMS simulator [32].

For a gate within $T$ logic levels of the affected gate, the electrical masking, i.e. attenuation of the pulse width and amplitude, must be taken into account. It has been observed that the impact of electrical masking is insignificant after the first two logic levels (see Figure 2), and the limit $T = 2$ is a common choice [33]. Hence, no detailed electrical analysis is required for the pulses on the gates beyond $T$ logic levels from the gate struck by the particle.

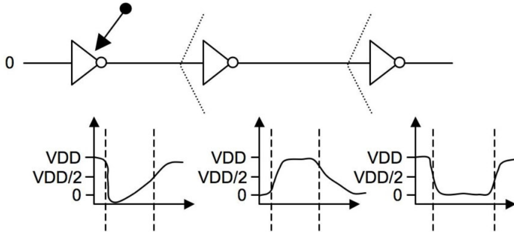


Fig. 2. SET waveform at fault site, after one and two gate levels

The SET characterization table contains an entry for each tuple $\{val, ttl, [fanout_1, \ldots, fanout_{ttl}], F\}$. $val$ denotes the logic value at the considered node. $ttl \leq T$ is the number of logic levels between the gate struck by the particle and the considered node. $[fanout_1, \ldots, fanout_{ttl}]$ is a list of inverter equivalent fanout loads through which the pulse has been propagated. $F$ are the parameters of the particle strike such as input pattern, transistor node and injected charge. For each tuple, the characteristics of the pulse are stored in the SET characterization table.

*2) Gate-level simulation:* A large number of SET events is simulated by using a VHDL simulator. SETs with parameters given by a specified distribution are injected into the circuit VHDL description. Signals driven by the gate affected by the SET and all gates within $T$ logic levels of that gate are each assigned a signal descriptor, which references the information stored in the SET characterization table.

For the injection and immediate propagation, the pulse parameters are looked up in the SET characterization table and the pulse is injected accordingly. Pulses on all other signals (those farther than $T$ logic levels from the site of the SET) are propagated using standard VHDL mechanisms, which implicitly consider dynamic and static logical masking as well as latching-window masking. The simulation reports the proportion of the SETs which were propagated to at least one flip-flop within its latching window among all injected SETs.

### B. Results

Selective hardening was applied to IWLS 93 benchmarks [34] synthesized by SIS using "stamina" for state minimization, "jedi" for state coding and script.rugged for logic optimization.

Accurate analysis of the SER caused by single-event transients was performed on the resulting circuits. The SET characterization library was created for a primitive cell library in a 130 nm process. The simulation was run for 10 million SET injections. A pseudo-random input sequence was applied to the circuit's inputs.

For the gate hardening, we have selected the technique presented in [7]. In this technique, a gate is hardened by simply duplicating the gate and connecting its inputs and outputs to the same node (Fig. 3). If a transistor is struck in one of the gates, the other gate will significantly attenuate the glitch by driving the correct value and absorbing the collected charge. As we distinguish between flip-to-0 and flip-to-1 SETs, a gate may be hardened against one or both of possible SETs. In the hardened gate, this may be achieved by just duplicating the NMOS or PMOS network of the gate. From our experiments,

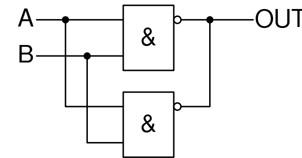


Fig. 3. Gate hardening by duplication [7]

we have determined the SET pulse widths and computed an average $LHF$ of 8. This value is consistent with [7].

The results are reported in Table I. The first column contains the number of possible faults $|C|$ in the circuit. Column '$t_c$'

quotes the clock cycle time in picoseconds. Column '$E_{ref}$' contains the number of fault injections which lead to an error effect manifestation in a flip-flop of the unhardened version of the circuit. The remaining $(1,000,000 - E_{ref})$ injected faults did not result in an observable effect due to either logical, latching-window or electrical masking. The subsequent columns report the results for hardened circuits with target $c$ set to 0.5 and 0.25, respectively. Columns '$|C_1|$' contain the number of faults selected for hardening. Columns '$E$' contain the number of injections which manifested themselves in a flip-flop while columns '$c_{exp}$' quote the percentage of such errors related to the number $E_{ref}$ of their counterparts in the unhardened circuit. '$c_{exp}$'=$E/E_{ref}$ is the experimental equivalent of the hardening target $c$.

It is obvious that the target $c$ for error reduction is reached indeed. In many cases, the measurements show better results than expected from $c$. This is caused by the higher probability of electrical masking of the shorter pulses injected at hardened gates. But especially for $c = 0.25$, the results are within very few percent of the target. Here, no more than 60% of the fault sites have to be hardened in any of the circuits.

Table II compares a purely topological hardening selection as proposed in [10] with the detection based solution presented here. In [10] gates are hardened which are rather close to the output latches. Columns 2 to 4, and 5 to 7 respectively, show $c_{exp} = E/E_{ref}$ if 10%, 20% or 50% of the faults are hardened according to each selection strategy. The experiment again uses $1,000,000$ SET injections. The number of resulting errors is omitted for brevity.

If the same amount of gates is hardened by using the algorithm presented here, significantly less errors are observed leading to a significant improvement of $c_{exp}$ in columns 5 to 7. Please note, that the strategy presented in [10] is based on the assumption that many SETs are very short and are always filtered after a few gate levels. Here, the gate level simulation takes electrical masking into account. But in general, the assumption is only valid if the circuit is completely protected from high-energy radiation. Furthermore, [9] has shown that SET width is underestimated by most electrical models. In contrast, the selective hardening presented here does not make any such assumptions and works in the general case.

| | Selection by topology | | | Presented selection | | |
|---|---|---|---|---|---|---|
| $\|C_1\|/\|C\| =$ | 10% | 20% | 50% | 10% | 20% | 50% |
| bbara | 82% | 75% | 62% | 60% | 51% | 24% |
| bbsse | 91% | 79% | 53% | 69% | 55% | 14% |
| cse | 88% | 69% | 40% | 35% | 20% | 12% |
| dk14 | 87% | 80% | 77% | 77% | 46% | 14% |
| dk15 | 76% | 73% | 48% | 70% | 44% | 19% |
| dk16 | 87% | 77% | 46% | 70% | 59% | 23% |
| dvram | 81% | 67% | 45% | 69% | 52% | 16% |
| ex6 | 97% | 86% | 52% | 72% | 44% | 19% |
| fetch | 86% | 75% | 55% | 69% | 38% | 16% |
| keyb | 68% | 59% | 39% | 43% | 31% | 14% |
| kirkman | 83% | 83% | 76% | 66% | 37% | 19% |
| nucpwr | 82% | 71% | 39% | 73% | 46% | 16% |
| opus | 98% | 98% | 87% | 65% | 38% | 20% |
| s1 | 83% | 70% | 54% | 59% | 43% | 17% |
| sand | 84% | 74% | 51% | 65% | 49% | 20% |
| styr | 92% | 89% | 52% | 39% | 23% | 11% |
| sync | 86% | 77% | 69% | 75% | 47% | 19% |
| tbk | 79% | 70% | 23% | 46% | 30% | 15% |

TABLE II

$c_{exp}$ WHEN HARDENING FOR GIVEN $|C_1|/|C|$

| Circuit | $C$ | $t_c$ [ps] | $E_{ref}$ | $c = 0.5$ | | | $c = 0.25$ | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $\|C_1\|$ | $E$ | $c_{exp}$ | $\|C_1\|$ | $E$ | $c_{exp}$ |
| bbara | 270 | 670 | 5417 | 26% | 2730 | 50% | 52% | 1310 | 24% |
| bbsse | 578 | 909 | 3725 | 19% | 2031 | 55% | 45% | 740 | 20% |
| cse | 952 | 1081 | 3178 | 15% | 730 | 23% | 34% | 490 | 15% |
| dk14 | 434 | 993 | 3184 | 30% | 989 | 31% | 60% | 417 | 13% |
| dk15 | 376 | 994 | 3521 | 27% | 1245 | 35% | 55% | 616 | 17% |
| dk16 | 1208 | 2068 | 1440 | 25% | 770 | 53% | 53% | 307 | 21% |
| dvram | 1038 | 932 | 4082 | 28% | 1650 | 40% | 54% | 592 | 15% |
| ex6 | 382 | 928 | 3024 | 28% | 1145 | 38% | 56% | 542 | 18% |
| fetch | 636 | 697 | 7915 | 23% | 2911 | 37% | 46% | 1395 | 18% |
| keyb | 1006 | 905 | 2370 | 13% | 929 | 39% | 33% | 474 | 20% |
| kirkman | 894 | 839 | 4256 | 20% | 1576 | 37% | 47% | 855 | 20% |
| nucpwr | 824 | 568 | 7671 | 24% | 2827 | 37% | 50% | 1146 | 15% |
| opus | 342 | 576 | 10255 | 18% | 4204 | 41% | 40% | 2228 | 22% |
| s1 | 594 | 1159 | 4446 | 24% | 1552 | 35% | 48% | 797 | 18% |
| sand | 2818 | 1186 | 83 | 17% | 30 | 36% | 36% | 19 | 23% |
| styr | 2250 | 2677 | 783 | 15% | 241 | 31% | 33% | 133 | 17% |
| sync | 1608 | 1403 | 5583 | 18% | 2897 | 52% | 34% | 1792 | 32% |
| tbk | 1206 | 1442 | 1447 | 9% | 686 | 47% | 24% | 373 | 26% |

TABLE I

SOFT ERROR RATE IMPROVEMENT BY PARTIAL HARDENING (1,000,000 SET)

## VI. Conclusions

We presented a method to select gates for hardening already at gate level before technology mapping. The method is based on detection probability analysis and allows to specify an error reduction factor which is obtained with minimum hardware overhead. Intensive, precise simulation with a refined soft error model verifies that the improvements are obtained indeed. Comparison with other selective hardening techniques show that the new approach needs significantly less overhead for obtaining the identical improvement.

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