Diagnosis of Realistic Defects Based on the X-Fault Model[*]

Ilia Polian[*]   Yusuke Nakamura[**]   Piet Engelke[*]   Stefan Spinner[*]

Kohei Miyase[**]   Seiji Kajihara[**]   Bernd Becker[*]   Xiaoqing Wen[**]

[*]Institute for Computer Science
Albert-Ludwigs-University
Georges-Köhler-Allee 51
D-79110 Freiburg i. Br., Germany
{engelke|stspinne|polian|becker}@informatik.uni-freiburg.de

[**]Faculty of Computer Science and Systems Eng.
Kyushu Institute of Technology
Iizuka-shi, 820-8502, Japan
yusuke.kyutech@gmail.com
{k_miyase|kajihara|wen}@cse.kyutech.ac.jp

Abstract

Defects not described by conventional fault models are a challenge for state-of-the-art fault diagnosis techniques. The X-fault model has been introduced recently as a modeling technique for complex defect mechanisms. We analyze the performance of the X-fault diagnosis for a number of defect classes leading to highly complex circuit behavior on electrical level. Experiments performed using accurate resistive-bridge and interconnect-open simulators demonstrate the superiority of X-fault diagnosis over traditional methods.

Keywords: Fault diagnosis, X-fault model, Resistive bridges, Interconnect opens

1 Introduction

Automatic defect diagnosis is a key component of a design-for-manufacturing (DFM) flow [1]. Diagnosis methods identify the site of the defect which has lead to a failure during test or at least narrow down the search for such sites to a few candidates [2–4]. Most of the methods assume that actual defects behave like single stuck-at faults. Modeling of defects by stuck-at faults is a standard assumption in the context of automatic test pattern generation (ATPG). This assumption often leads to reasonable ATPG results due to incidental detections of unmodeled defects by patterns generated for other faults.

Since diagnosis methods must derive the defect site based on the circuit responses only, they require a higher accuracy of the defect model used. Diagnosis based on the multiple stuck-at model or other fault models has been investigated in the past [5–7]. However, considering non-standard fault models in addition to the stuck-at fault model may lead to excessive increase in complexity, tester memory and test application time and thus elevated cost. This is particularly true for approaches which take complex defect behavior on electrical level into account [8]. As a possible remedy, diagnosis techniques which are based on non-standard fault models but

use only stuck-at data have been explored in [9, 10]. These approaches typically cannot achieve high diagnostic resolution.

The X-fault model [11] enables diagnosis which combines the efficiency of techniques based on stuck-at faults with excellent diagnostic resolution and does not require modeling at electrical level. Possible defect behaviors are represented by logic values and symbolic simulation is performed. High effectiveness of this diagnosis approach for Byzantine defects (defined as multiple stuck-at faults on several fanout branches of the same logic signal) has been demonstrated in [11].

In this paper, we investigate the performance of diagnosis based on X-fault model for hard-to-diagnose defect classes. We inject resistive bridges [12] and interconnect opens [8] into benchmark circuits, determine responses using simulators from [13, 14], apply the diagnosis procedure and determine whether the injected defect was identified. Both defect classes considered pose substantial challenges for any diagnosis approach which will be outlined below. In this study, we consider only static defects. This is consistent with diagnosis being applied to the responses collected during (static) scan test. Diagnosis of delay faults (e.g., due to resistive open defects) is a topic of future research.

In case of resistive bridges, two lines are involved in a defect. Depending on the bridge resistance R_{sh}, the defect may induce voltage levels close to the logic thresholds of the gates driven by the bridged lines. Hence, different gates may interpret the same voltage differently (as logic-0 or logic-1). Furthermore, the voltage depends on the values at the gates which drive the bridged lines. For example, if one bridged line is driven by a NAND gate, the logical values interpreted by the gates driven by the line may depend on whether the NAND gate sees 00 or 01 at its inputs, although the logical value on the line is 1 in both cases. Hence, it is impossible to determine a (multiple) stuck-at fault which is equivalent to a resistive bridge as the behavior is pattern-dependent.

For interconnect opens, we employ the aggressor-victim model used in [8]. We assume that an interconnect is divided

---

into two parts by an open defect and that only one part is still being driven by the gate at its source and the other part is floating. The voltage on the floating part of the interconnect is determined by the logical value of aggressors, i.e., neighbor interconnects with non-zero parasitic cross-capacitance to the defective interconnect. Aggressors connected with V_{DD} (power supply rails and signal interconnects having the logical value of 1 under the current pattern) attempt to induce logic-1 on the floating part. Aggressors connected with ground (ground rails and signal interconnects having the logical value of 0 under the current pattern) attempt to induce logic-0 on the floating part.

According to the model from [8], the voltage on the floating part is interpreted as logic-1 if the number of aggressors connected with V_{DD} weighted by the parasitic cross-capacitance of each aggressor exceeds the same number calculated for aggressors connected with ground. This voltage is interpreted as logic-0 otherwise. Similar to the Byzantine model, the fanout affected by the defect depend on the exact location of the open defect within the topology of the interconnect. The challenge for diagnosis derives from the fact that, although only one line is affected, its value depends on a large number of aggressors distributed all over the circuit. Furthermore, the line may behave as stuck-at-0 and as stuck-at-1 under different patterns.

The behavior of the circuit with a resistive bridge or an interconnect open depends on electrical parameters such as the widths and the lengths of the transistor in the gates, the threshold voltages and the capacitances between interconnects. The simulators used for the analysis take all these data into account. On the other hand, X-fault diagnosis does not use electrical-level information. This simplifies the application of this method in flows where electrical information is not available for any reason, e.g., intellectual property protection.

The remainder of the paper is organized as follows. The next section gives an overview of the X-fault diagnosis methodology. Experimental results for resistive bridging faults and preliminary results for interconnect open faults are reported in Section 3. Section 4 concludes the paper.

2 X-Fault Diagnosis

X-fault diagnosis takes fail data (responses of a circuit observed on the test equipment) as input and produces a list of *multiplets* sorted by their *score*. A multiplet is a collection of *X-faults* which explains the circuit failure to some degree. As will be described later, one X-fault is associated with potential failure at one signal line (fanout stem or fanout branch). A multiplet consisting of n X-faults suggests that the physical defect is related to the signal lines corresponding to that X-faults. The diagnosis algorithm calculates, for each multiplet, its score. A multiplet's score gives the confidence of the diagnostic algorithm that the failure is explained by the multiplet. Given two multiplets, the multiplet with a higher score is more likely to explain the failure.

The X-fault model describes erroneous behavior on signal lines. It accounts for pattern-dependent and Byzantine behavior, i.e., values on different fanout branches of the same signal line being interpreted as different logical values by different gates and under different test patterns. In addition, it does not require low-level electrical information. For a fanout-free signal line, an X-fault results in the inversion of the fault-free value on the line. For a line with m fanout branches, m symbolic variables X_1 through X_m are defined and assigned to the branches. Variables X_1 through X_m may assume any logical value (0 or 1) independent from each other.

To check whether an X-fault explains a failing test pattern, X-fault simulation is performed. For a fanout-free line, the fault-free value on this line is inverted and the resulting values on the output of the circuit are compared with the observed responses. For a line with m fanout branches, the simulation algorithm tries to find an assignment to variables X_1 through X_m which implies output values compatible with the responses measured by the test equipment. While the naive approach (assigning all possible logical value combinations to X_1 through X_m) requires 2^m simulation runs, optimized X-propagation and X-resolution techniques reduce the number of simulations needed in practice [11]. For instance, values X_i which are not propagated to an output due to a lack of a sensitized path are excluded from consideration.

The likelihood that an X-fault f explains a failing test pattern t is quantified by the *diagnosis value* $p(f, t)$. To calculate $p(f, t)$, circuit responses (values on the outputs) P_1 through P_k are obtained by simulation, where one P_i corresponds to one assignment to symbolic variables X_1 through X_m. For an X-fault on a fanout-free line, k equals 1. The match $p(f, t, P_i)$ between P_i and the responses observed on the test equipment is calculated for each P_i.

To increase the probability of a successful matching, only outputs $Reach\_PO(f)$ structurally reachable from the location of the candidate X-fault f are considered when computing $p(f, t, P_i)$. Furthermore, the *level* $L(f)$ of the fault f, i.e., the length of the longest path from the location of f to an output, is taken into account. Faults with a higher level are more likely to explain a physical defect if the simulated responses match the responses observed on the test equipment.

The match between P_i and the observed responses is calculated as

$$p(t, f, P_i) = \frac{L(f)}{L_{\max}} \cdot \frac{|Error\_PO(t) \cap Reach\_PO(f)|}{|Reach\_PO(f)|} \tag{1}$$

if P_i matches with the responses observed on the test equipment for test pattern t on outputs in $Reach\_PO(f)$, and 0 otherwise. In (1), $L_{\max}$ stands for the maximal level of any fault in the circuit and $Error\_PO(t)$ denotes the outputs on which erroneous values have been observed for test pattern t. The diagnosis value is obtained by

$$p(t, f) = p(t, f, P_1) + \cdots + p(t, f, P_k). \tag{2}$$

For a test set $T = \{t_1, \ldots, t_l\}$, the *average diagnostic value* $p(T, f) = (p(t_1, f) + \cdots + p(t_l, f))/l$ is computed.

Circuit	Multiplets	Match	Rank	ES	≤ 5	≤ 10
c5315	350.42	95	19.68	4.88	56	61
c6288	568.93	98	23.52	1.17	32	47
c7552	630.37	95	19.82	5.63	45	54
cs15850	94.60	97	4.21	13.07	82	90
cs38417	121.18	100	4.99	3.88	80	90
cs38584	44.23	100	2.77	2.75	89	97

Table 1: X-fault diagnosis for 100 resistive bridging faults

Circuit	Multiplets	Match	Rank	ES	≤ 5	≤ 10
c5315	27771.58	92	100.55	16.86	39	49
c6288	947.45	98	43.93	1.77	34	49
c7552	1640.03	97	494.04	12.94	35	42
cs15850	116.84	95	5.76	19.05	80	88
cs38417	163.15	90	15.77	12.00	63	78
cs38584	101.86	98	4.71	4.97	72	87

Table 2: Stuck-at fault diagnosis for setup of Table 1

Circuit	Match	Rank		≤ 5		≤ 10	
		X	s@	X	s@	X	s@
c5313	88	20.40	104.41	54	38	58	46
c6288	98	23.52	43.94	32	34	47	49
c7552	93	20.22	510.88	43	34	52	40
cs15850	92	4.00	5.72	80	79	86	86
cs38417	90	5.43	15.77	70	63	80	78
cs38584	90	2.73	4.71	88	72	95	87

Table 3: Comparison of X-fault and stuck-at fault diagnosis of resistive bridging faults

A multiplet can be calculated as a collection of X-faults such that, for every failing test pattern t, the multiplet contains at least one X-fault f with $p(t, f) > 0$. The score of a multiplet is the sum of average diagnostic values of X-faults included in the multiplet.

3 Experimental Results

3.1 Experimental setup

To evaluate the effectiveness of X-fault based diagnosis for complex non-target defects, we injected resistive bridging faults and interconnect open faults into ISCAS 85 and combinational parts of ISCAS 89 circuits. Resistive bridging faults and interconnect open faults are used as surrogates for physical defects. By using this approach, no manufacturing of actual silicon is required. Moreover, diagnosis quality is easier to evaluate than in a hardware experiment. In our simulation study, we can simply compare the defect locations yielded by the diagnosis method with the locations on which the faults were inserted. In a hardware experiment, sophisticated and costly failure analysis would have been necessary to verify whether the reported defect locations are indeed defect sites.

The quality of a diagnosis procedure is quantified by its ability to find the defective locations in the circuit. In methods such as X-fault diagnosis, which produce a number of alternative solutions (multiplets), the *rank* of the correct solution (i.e., multiplet which contains the actual defective location) in the sorted list of multiplets, is also important. The underlying assumption is that the diagnostic information may be used for physical failure analysis (P-FA). The FA engineer will perform time-consuming and potentially destructive operations (deprocessing, probing, chemical analysis, etc.) starting with the first defect location in the list, stopping when the defect has been found. Hence, less effort will be spent if the correct defect location is close to the list's beginning. Recall that the multiplets derived by X-fault diagnosis are sorted by their score as defined above.

3.2 Results for resistive bridging faults

Diagnosis results for 100 resistive 2-line bridging faults are summarized in Table 1. The signal lines involved in the faults were selected randomly. The bridge resistance R_{sh} was also picked randomly, however we made sure that (1) the fault is not redundant, i.e., does expose faulty behavior for some test pattern and (2) higher R_{sh} values are chosen with a higher probability. The latter condition ensures that the fault is likely to lead to non-trivial Byzantine behavior which is difficult to diagnose.

The selected faults were simulated under stuck-at test patterns using the simulator from [13] and assuming 0.35 μm technology parameters by austriamicrosystems. The calculated circuit responses were handed to the X-fault diagnosis routine as a surrogate of responses observed on the test equipment.

The average number of multiplets, i.e., alternative solutions found by the diagnosis algorithm, is reported in column 2 of Table 1. The number of X-faults contained in any multiplet (not reported) was 1 or 2 for almost all multiplets. Column 3 gives the number of resistive bridging faults which were matched, i.e., for which at least one of the signal lines involved in the bridge is contained in at least one multiplet.

Column 4 reports the average rank of the first multiplet in the sorted list in which one of the bridged lines shows up. Since some multiplets have identical score, this rank is not unique. The average number of multiplets with a score equal to that of the first matching multiplet can be found in column 5 ('ES' stands for 'equal score'). The final two columns report the number of faults for which the matching multiplet was among top 5 and top 10 multiplets in the sorted list, respectively.

It can be seen that resistive bridging faults indeed pose a severe challenge to the diagnosis algorithm. The number of multiplets generated and the rank are higher than in previous work [11]. This particularly holds for ISCAS 85 circuits with complex structure, long paths and large number of reconvergencies.

The same experiment was repeated using the same test patterns but stuck-at fault diagnosis instead of X-fault diagnosis. The results are reported in Table 2. X-fault diagnosis outperforms stuck-at fault diagnosis in number of matches, average rank and number of matched faults among top 5 and top 10 multiplets.

To accurately compare X-fault diagnosis and stuck-at fault diagnosis, we repeated the experiments considering

Circuit	Test set	Method	Multiplets	Match	Rank	ES	≤ 5	≤ 10
c3540	1-det.	X-fault	31.03	99	8.00	2.16	67	81
c3540	1-det.	stuck-at	498.45	70	9.13	4.24	46	53
c6288	1-det.	X-fault	11.46	101	4.53	1.17	76	88
c6288	1-det.	stuck-at	249.34	75	5.59	1.43	51	63
c6288	5-det.	X-fault	5.48	101	1.13	2.62	101	101
c6288	5-det.	stuck-at	44.48	74	3.03	1.31	65	73
c6288	10-det.	X-fault	4.89	101	2.39	1.13	96	101
c6288	10-det.	stuck-at	7.90	74	2.78	1.31	69	73
c7552	1-det.	X-fault	28.24	101	10.53	2.71	61	75
c7552	1-det.	stuck-at	156.95	79	93.14	4.97	44	51
c7552	5-det.	X-fault	30.62	101	7.59	2.05	66	79
c7552	5-det.	stuck-at	82.64	79	10.77	3.46	45	52
c7552	10-det.	X-fault	29.45	101	13.63	1.95	65	78
c7552	10-det.	stuck-at	56.60	78	10.09	3.22	44	51

Table 4: Comparison of X-fault and stuck-at fault diagnosis of 101 interconnect open faults

only faults for which both X-fault diagnosis and stuck-at fault diagnosis found at least one match. Table 3 summarizes the results. The number of considered faults is given in the second column. The average rank and the number of matched faults among top 5 and top 10 multiplets are consistently better for X-fault diagnosis (denoted by 'X') than for stuck-at fault diagnosis (denoted by 's@').

3.3 Preliminary results for interconnect opens

We applied X-fault diagnosis and stuck-at fault diagnosis methods to 101 interconnect open faults in ISCAS 85 circuits. The flow was similar to that used for the resistive bridging faults, but the interconnect open simulator from [14], which is based on the model from [8], was employed instead of the resistive bridging fault simulator. The circuits were laid out and the parasitic capacitances needed to simulate the interconnect open defects were extracted by the flow described in [15].

Table 4 contains the results. Although X-fault diagnosis outperforms stuck-at fault diagnosis, the achieved average rank is generally lower than expected. A recent extension of the X-fault diagnosis flow [16] demonstrated that the performance of the X-fault diagnosis for open defects increases significantly if the exact topology of the interconnect is taken into account. In the future, we will design a methodology to supply this information from our layout database to the diagnosis tool. We expect the achieved rank to improve by approximately factor 2 as reported in [16] for a simpler open defect model.

4 Conclusions

X-fault diagnosis is a technology which works on gate level and abstracts from low-level electrical data. We showed that, despite this, X-fault diagnosis is able to generate high-quality diagnostic solutions for defect classes with highly non-trivial electrical behavior: resistive bridging faults and interconnect open faults, clearly outperforming stuck-at fault diagnosis. Even though the absolute performance figures, in particular the average rank, may look worse than typical results for diagnosing stuck-at faults, one needs to keep in mind that the considered defect types are generally difficult to diagnose by any method and they only account for a limited fraction of the total defect population. In reality, the presence of a large number of easy-to-diagnose defects will improve the average rank. Nevertheless, methods to improve the effectiveness of diagnosis for hard-to-diagnose defects are still desirable.

One possible direction for future research would be the integration of low-level electrical data into the diagnostic method. Taking the topology of the interconnect into account is one first step in this direction. Generally, the integration must not compromise scalability and may only require data which can be obtained easily. The understanding of the trade-off between the accuracy of the diagnosis and its complexity should be enhanced to find an optimal approach in a given environment. The application of the method to large industrial circuits with particularities such as tri-state buses is another area in which research is needed.

5 References

[1] H. Tang, S. Manish, J. Rajski, M. Keim, and B. Benware. Analyzing volume diagnosis results with statistical learning for yield improvement. In *European Test Symp. 2007*, pages 145–150, 2007.

[2] J.M. Galey, R.E. Norby, and J.P. Roth. Techniques for the diagnosing of switching circuit failures. In *Symp. on Switching Circuit Theory and Logical Design*, pages 152–160, March 1961.

[3] W.H. Kautz. Fault testing and diagnosis in combinational digital circuits. *IEEE Trans. on Comp.*, C-17(4):352–366, 1968.

[4] J. Waicukausli and E. Lindbloom. Failure diagnosis of structured VLSI. *IEEE Design & Test of Comp.*, pages 49–60, 1989.

[5] A. D. Friedman. Diagnosis of short-circuit faults in combinational logic circuits. *IEEE Trans. on Comp.*, C-23(7):746–752, July 1974.

[6] M. Abramovici and M.A. Breuer. Multiple fault diagnosis in combinational circuits based on an effect-cause diagnosis. *IEEE Trans. on Comp.*, C-29(6):451–460, 1980.

[7] H. Cox and J. Rajski. A Method of Fault Analysis for Test Generation and Fault Diagnosis. *IEEE Trans. on CAD*, 7(7):813–833, July 1988.

[8] Y. Sato, I. Yamazaki, H. Yamanaka, T. Ikeda, and M. Takakura. A persistent diagnostic technique for unstable defects. In *Int'l Test Conf.*, pages 242–249, 2002.

[9] S.D. Millman, E.J. McCluskey, and J.K. Acken. Diagnosing CMOS bridging faults with stuck-at fault dictionaries. In *Int'l Test Conf.*, pages 860–870, 1990.

[10] D.B. Lavo, B. Chess, T. Larrabee, and F.J. Ferguson. Diagnosis of realistic bridging faults with single-stuck-at information. *IEEE Trans. on CAD*, 17(3):255–268, 1998.

[11] X. Wen, T. Miyoshi, S. Kajihara, L.-T. Wang, K.K. Saluja, and K. Kinoshita. On per-test fault diagnosis using the X-fault model. In *Int'l Conf. on CAD*, pages 633–640, 2004.

[12] M. Renovell, P. Huc, and Y. Bertrand. The concept of resistance interval: A new parametric model for resistive bridging fault. In *VLSI Test Symp.*, pages 184–189, 1995.

[13] P. Engelke, I. Polian, M. Renovell, and B. Becker. Simulating resistive bridging and stuck-at faults. *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 25(10):2181–2192, Oct. 2006.

[14] S. Spinner, I. Polian, P. Engelke, B. Becker, M. Keim, and W.-T. Cheng. Automatic test pattern generation for interconnect open defects. In *VLSI Test Symp.*, 2008. In press.

[15] S. Spinner, J. Jiang, I. Polian, P. Engelke, and B. Becker. Simulating open-via defects. In *Asian Test Symp.*, pages 265–270, 2007.

[16] X. Wen, Y. Yamato, K. Miyase, S. Kajihara, H. Furukawa, L.-T. Wang, K.K. Saluja, and K. Kinoshita. An improved method of per-test X-fault diagnosis for deep-submicron LSI circuits. In *Workshop on RTL and High Level Testing*, pages 55–60, 2006.