On Detection of Resistive Bridging Defects by Low-Temperature and Low-Voltage Testing

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***Abstract*—Test application at reduced power supply voltage (low-voltage testing) or reduced temperature (low-temperature testing) can improve the defect coverage of a test set, particularly of resistive short defects. Using a probabilistic model of two-line nonfeedback short defects, we quantify the coverage impact of low-voltage and low-temperature testing for different voltages and temperatures. Effects of statistical process variations are not considered in the model. When quantifying the coverage increase, we differentiate between defects missed by the test set at nominal conditions and undetectable defects (flaws) detected at nonnominal conditions. In our analysis, the performance degradation of the device caused by lower power supply voltage is accounted for. Furthermore, we describe a situation in which defects detected by conventional testing are missed by low-voltage testing and quantify the resulting coverage loss. Experimental results suggest that test quality is improved even if no cost increase is allowed. If multiple test applications are acceptable, a combination of low voltage and low temperature turns out to provide the best coverage of both hard defects and flaws.**

***Index Terms*—Early life failures, low-temperature testing, low-voltage testing, resistive short defects.**

I. Introduction

APPLYING test patterns at reduced power supply voltage and/or reduced temperature is known to be effective in identifying defective ICs which have passed conventional test. The extended defect detection capabilities of low-voltage testing have been demonstrated in a silicon experiment [1], a mathematical analysis [2], a SPICE analysis [3], and a simulation experiment [4]. Low-voltage testing is sometimes also called very-low-voltage (VLV) testing. A technique related to low-voltage testing is called MinVDD [5]. The effectiveness of low-temperature testing has been demonstrated for three (real) defect classes at Intel [6] and was investigated on a fabricated silicon for resistive salicide, i.e., $TiSi_2$, which is used to enhance the conductivity of polycrystalline silicon, in [7]. It has also been applied successfully in combination with IDDQ testing [8]. In addition, low-voltage and low-temperature testing have been reported to detect flaws in the so-called weak ICs, i.e., defects resulting in infant mortality, reduced reliability, or transient faults, rather than catastrophic failures [1]. These failures can become catastrophic in the future due to aging processes such as gate-oxide breakdown, hot carrier effects, and electromigration [9], [10]. Alternative methods for detecting flaws, such as burn-in, are often associated with considerable costs.

While low-temperature testing is associated with additional equipment cost, low-voltage testing is a low-cost technique. However, the frequency at which test patterns are applied must be reduced because the switching speed of the transistors decreases. This results in an increase of test-application time if the same number of test patterns is applied. On the other hand, if the available test-application time is fixed, the application of the complete test set will become impossible.

In this paper, we study the effects of low-voltage testing, low-temperature testing, and their combination on detection of resistive shorts which are a major class of defects resulting in flaws. For simplicity, we refer to test application using either reduced power supply voltage V_{DD}, reduced temperature T or both as testing under non-nominal conditions, or low-X testing.

If a short defect with a certain resistance is detected by the low-X testing but not by testing at nominal conditions, this can have two reasons. First, this particular defect could have been detectable at nominal conditions, but it was not detected because the coverage of the test set was insufficient, i.e., none of the test vectors that activate the defect and propagate its effect to an output sets the inputs of the gates driving the shorted lines to values which are required to detect the maximum short resistance. In this case, the low-X testing "increased" the coverage of this test set. The second possible reason is that the short resistance is too high to be detected by any test pattern at nominal conditions. Such a defect might be considered "redundant" and, thus, irrelevant. On the other hand, various aging mechanisms previously outlined are likely to aggravate the defect; therefore, the IC in question will fail the burn-in test or become an early life failure. At least in some applications, these "weak" ICs must be rejected.

In this paper, we quantify the impact of low-X testing on resistive-bridging-fault (RBF) coverage. This allows us not only to decide whether the low-X testing as such is beneficial but also to suggest the best V_{DD} and T values in testing a given

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circuit. We consider two scenarios: Scenario **CN** (cost neutral) and Scenario **AS** (additional screen). Under Scenario **CN**, we assume that additional costs due to the low-X testing are unacceptable. In particular, no test-time increase is tolerated. As a consequence, we assume that the low-X testing is performed instead of testing at nominal conditions. When V_{DD} is lowered, the operating frequency of the device is reduced such that not all vectors of the test set can be applied. We determine whether and when applying additional test patterns at nominal V_{DD} yields better defect coverage than applying the test set at reduced voltage (and, thus, at reduced frequency). Furthermore, we consider only low-voltage testing because low-temperature testing is associated with additional costs for the equipment to control the temperature such as a thermal chuck. In contrast, low-voltage testing does not require any additional equipment cost. Scenario **CN** is designed to reflect the requirements of high-volume manufacturing test.

In contrast, Scenario **AS** assumes a product with elevated reliability requirements for which thorough testing at increased cost is tolerable. Under Scenario **AS**, the IC is tested twice: first under nominal conditions and then using the low-X testing. Both V_{DD} and T can be lowered. All vectors of a test set are applied in both test runs, irrespective of any performance degradation.

To quantify the effects of the low-X testing on RBF detection, we enhance the RBF model from [11]–[13] by voltage-dependence and temperature-dependence models. The models are based on resistance interval propagation, thus allowing us to determine the fault coverage taking into account all possible bridge defect resistances from 0 Ω to infinity (rather than considering some fixed values). We account for the effects of V_{DD} and T on transistor parameters and also the temperature-induced change of the bridge resistance. We introduce metrics for quantifying RBF coverage under nominal and low-X conditions, accounting for a performance degradation under Scenario **CN**. We distinguish the analysis of the undetected defects detected by the low-X testing (i.e., those for which a test theoretically exists) from the analysis of the undetectable defects detected by the low-X testing, which correspond to flaws and are likely to result in reliability issues. Experimental results are obtained by an enhanced version of the simulator from [16]. We also demonstrate an example for which low-voltage testing, contrary to the conventional wisdom, actually leads to a coverage loss, and then, we quantify its extent.

The remainder of this paper is organized as follows. The extensions of the RBF model from [11], [13], [16], and [18] to the low-X testing are presented in Section II. This includes metrics to quantify the impact of the low-X testing, the effects of performance degradation, and the voltage-dependence and the temperature-dependence models. The voltage-dependence model is required for both Scenarios **CN** and **AS**, the performance degradation is only considered under Scenario **CN**, and the temperature-dependence model is only used for Scenario **AS**. In Section III, experimental results for both Scenarios **CN** and **AS** are reported. Section IV gives an example for coverage loss through low-voltage testing, introduces a metric, and reports experimental data on such loss. Section V concludes this paper.

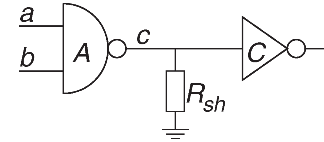


Fig. 1. Example circuit.

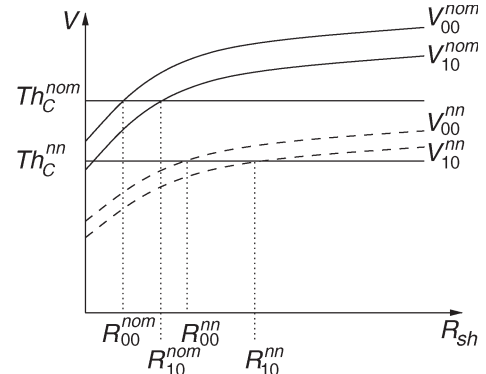


Fig. 2. $R_{\mathrm{sh}}-V$ diagram.

II. RBF Detection Under Nonnominal Conditions

A. RBF Model Under Nominal Conditions

The example circuit in Fig. 1 has a resistive stuck-at-zero fault on line c, i.e., a resistive short to ground.[1] The short resistance is denoted by R_{sh}. If the applied pattern is "00," then two p transistors from the pull-up network of the gate A drive the line c. In Fig. 2, a possible voltage characteristic of line c as a function of R_{sh} for a nominal V_{DD} and a test pattern "00" is shown as V_{00}^{nom} (it is the uppermost curve in the figure).

In accordance with previous works, we assume that the gate C has an exact-defined threshold voltage $\mathrm{Th}_C^{\mathrm{nom}}$. All voltages above $\mathrm{Th}_C^{\mathrm{nom}}$ are interpreted as the logical value of one, and any voltage below is interpreted as logic 0. In Fig. 2, $\mathrm{Th}_C^{\mathrm{nom}}$ is shown as a horizontal line because it does not depend on R_{sh}. The value R_{00}^{nom} is called critical resistance. The short defect is detected only for the R_{sh} values within the interval $[0\,\Omega, R_{00}^{\mathrm{nom}}]$, which is called the analog detectability interval (ADI). The ADI is defined with respect to a defect (here, resistive stuck-at zero at c), a test pattern (here, "00"), and V_{DD} and T (here, nominal).

The voltage characteristic for pattern "10" is shown in Fig. 2 as V_{10}^{nom}. Its ADI $[0\ \Omega, R_{10}^{\mathrm{nom}}]$ contains the ADI for the test pattern "00." The pattern "01" leads to an identical situation: $R_{10}^{\mathrm{nom}} = R_{01}^{\mathrm{nom}}$. The pattern "11" does not detect the defect: There is no critical resistance, and the ADI is empty.

Given a test set, the C-ADI is defined as the union of ADIs of individual vectors (C stands for "covered by the test set"). For instance, the C-ADI of the test set {"00", "11"} is given as $[0\ \Omega, R_{00}^{\mathrm{nom}}] \cup \emptyset = [0\ \Omega, R_{00}^{\mathrm{nom}}]$. G-ADI (global) is defined as the C-ADI of the exhaustive test set; in our example, it is $[0\ \Omega, R_{10}^{\mathrm{nom}}]$. G-ADI can be calculated exactly by either exhaustive fault simulation [16] or a method based

[1]It would be possible to use a circuit with an RBF for illustration purposes. This would necessitate adding another line and further gates and considering the voltage of this second line. The electrical modeling would remain largely the same. As this would add complexity rather than insight, we decided to use the somewhat less studied resistive stuck-at fault in our example.

on a solver for Boolean satisfiability (SAT) problems [17] or can be approximated by locally exhaustive simulation [15], [16]. The exhaustive fault simulation is only feasible for small blocks, whereas the method from [17] has a complexity which is similar to automatic test-pattern generation for the stuck-at faults. The locally exhaustive simulation ignores logical constraints in the circuit and may result in overapproximation of the G-ADI (see [16] for data on the extent of that overapproximation).

In our example, G-ADI is $[0\ \Omega, R_{10}^{\mathrm{nom}}]$. The fault coverage can be defined as

$$\mathrm{FC} = 100\% \cdot \left(\int\limits_{C\text{-ADI}} \rho(r)dr \right) \Bigg/ \left(\int\limits_{G\text{-ADI}} \rho(r)dr \right) \quad (1)$$

where $\rho(r)$ is the probability density function of the short resistance r extracted from the manufacturing data (e.g., using a method from [20]). Thus, C-ADI and G-ADI are "weighted" by ρ in order to account for the short defects that are more likely to occur than others. There are several alternative fault-coverage definitions (see [16] for a discussion).

Statistical process variations may result in voltage characteristics and thresholds of the gates in a manufactured IC being different from their values in the electrical model. As a consequence, the critical resistances, the ADIs, and the fault coverages may also vary among the circuits. The model used in this paper does not incorporate the effects of statistical process variations. We note, however, that the critical resistances are likely to vary monotonically, i.e., if a critical resistance in the manufactured circuit is larger than in the model, then other critical resistances in the circuit are probably also larger than their counterparts in the model. Since the boundaries of C-ADI and G-ADI are critical resistances, C-ADI and G-ADI in the circuit are likely to either both increase or both decrease compared with the model. Since the fault coverage is calculated as the fraction of integrals over C-ADI and G-ADI, the monotonicity implies that, in many instances, the impact of process variations on actual fault coverage will be limited.

B. Metrics for Detection Under Nonnominal Conditions

The basic RBF model assumes that testing is performed under the conditions that the device will be exposed to during operation. However, it is possible to run the test under a different power supply voltage V_{DD} and/or temperature T. In general, the range of detected defects will shift due to changes in V_{DD} and T. In terms of the RBF model, the detection intervals C-ADI and G-ADI will change. We denote C-ADI and G-ADI under nominal conditions as C^{nom} and G^{nom}, respectively, and their counterparts under nonnominal conditions as C^{nn} and G^{nn}, respectively.[2] C^{nn} and G^{nn} can be calculated using the same procedures as C^{nom} and G^{nom} if the electrical RBF model is modified appropriately. We will describe the required modifications in Section II-D.

[2]In this paper, we assume circuits with one nominal voltage. Circuits that employ dynamic voltage scaling (DVS) must work reliably under multiple voltages. Our framework can be easily extended to DVS circuits. Results on testing the DVS circuits have been reported in [21].

For instance, consider low-voltage testing of the circuit from Fig. 1. The voltage characteristics for the reduced power supply voltage (V_{00}^{nn} for the test pattern "00" and V_{10}^{nn} for "10") are shown in Fig. 2 as dashed lines. The reduced threshold is shown as the horizontal line $\mathrm{Th}_C^{\mathrm{nn}}$. C^{nn} of the test set {"00", "11"} is $[0\ \Omega, R_{00}^{\mathrm{nn}}]$, and G^{nn} is $[0\ \Omega, R_{10}^{\mathrm{nn}}]$.

Both C-ADI and G-ADI have been enlarged by reducing the voltage, which is in line with the results in [1]–[3]. Moreover, in this example, C^{nn} is a superset of G^{nom}. This means that the (suboptimal) test set applied at reduced V_{DD} succeeds to detect every defect that is detectable at the nominal V_{DD}. Furthermore, it detects some flaws, namely, the short defects with resistances between R_{10}^{nom} and R_{00}^{nn}.

In order to quantify both effects, we propose three metrics: the nonnominal fault coverage, the combined fault coverage, and the flaw coverage $\mathrm{FC}_{\mathrm{flaw}}^{\mathrm{nn}}$. When considering the defects detected by nonnominal testing ($R_{\mathrm{sh}} \in C^{\mathrm{nn}}$), we distinguish between the defects that are detectable by static (e.g., scan) testing under nominal conditions ($R_{\mathrm{sh}} \in G^{\mathrm{nom}}$) and the defects that are not detectable by static testing under nominal conditions ($R_{\mathrm{sh}} \in [0\ \Omega, \infty] \setminus G^{\mathrm{nom}}$). The second category includes defects that are detectable by delay testing only, latent defects which might deteriorate and lead to early life failures [10], and redundant defects. In accordance to the literature, we refer to the first category as hard defects and the second category of defects as flaws [1].

A hard defect is detected by nonnominal (low-X) testing if $R_{\mathrm{sh}} \in C^{\mathrm{nn}} \cap G^{\mathrm{nom}}$ (if $R_{\mathrm{sh}} \notin G^{\mathrm{nom}}$, then the defect is not a hard defect). The nonnominal fault coverage $\mathrm{FC}^{\mathrm{nn}}$ relates all hard defects detected by the low-X testing to all hard defects, i.e., defects that are detectable under nominal conditions

$$\mathrm{FC}^{\mathrm{nn}} = 100\% \cdot \frac{\int_{(C^{\mathrm{nn}} \cap G^{\mathrm{nom}})} \rho(r)dr}{\int_{G^{\mathrm{nom}}} \rho(r)dr}. \quad (2)$$

While $\mathrm{FC}^{\mathrm{nn}}$ gives the probability that a hard defect is detected by the low-X testing alone, the combined fault coverage $\mathrm{FC}_{\mathrm{comb}}^{\mathrm{nn}}$ gives the probability that a defect is detected by either nominal or low-X testing, i.e., it has a resistance $R_{\mathrm{sh}} \in (C^{\mathrm{nom}} \cup C^{\mathrm{nn}}) \cap G^{\mathrm{nom}}$ (recall that $C^{\mathrm{nom}} \subset G^{\mathrm{nom}}$)

$$\mathrm{FC}_{\mathrm{comb}}^{\mathrm{nn}} = 100\% \cdot \frac{\int_{((C^{\mathrm{nom}} \cup C^{\mathrm{nn}}) \cap G^{\mathrm{nom}})} \rho(r)dr}{\int_{G^{\mathrm{nom}}} \rho(r)dr}. \quad (3)$$

The $\mathrm{FC}^{\mathrm{nn}}$ reflects the coverage of one test run at nonnominal conditions assumed in Scenario **CN**. The $\mathrm{FC}_{\mathrm{comb}}^{\mathrm{nn}}$ reflects the coverage of two test runs: one at nominal condition and one at nonnominal condition, which corresponds to Scenario **AS**.

For the flaws, i.e., the defects that are undetectable under nominal conditions, $R_{\mathrm{sh}} \in [0\ \Omega, \infty] \setminus G^{\mathrm{nom}}$ holds. The condition for a defect to be detected by nonnominal testing is $R_{\mathrm{sh}} \in ([0\ \Omega, \infty] \setminus G^{\mathrm{nom}}) \cap C^{\mathrm{nn}}$. We define the flaw coverage as the probability that a flaw is detected by nonnominal testing

$$\mathrm{FC}_{\mathrm{flaw}}^{\mathrm{nn}} = 100\% \cdot \frac{\int_{(([0\ \Omega, \infty] \setminus G^{\mathrm{nom}}) \cap C^{\mathrm{nn}})} \rho(r)dr}{\int_{[0 \Omega, \infty] \setminus G^{\mathrm{nom}}} \rho(r)dr}. \quad (4)$$

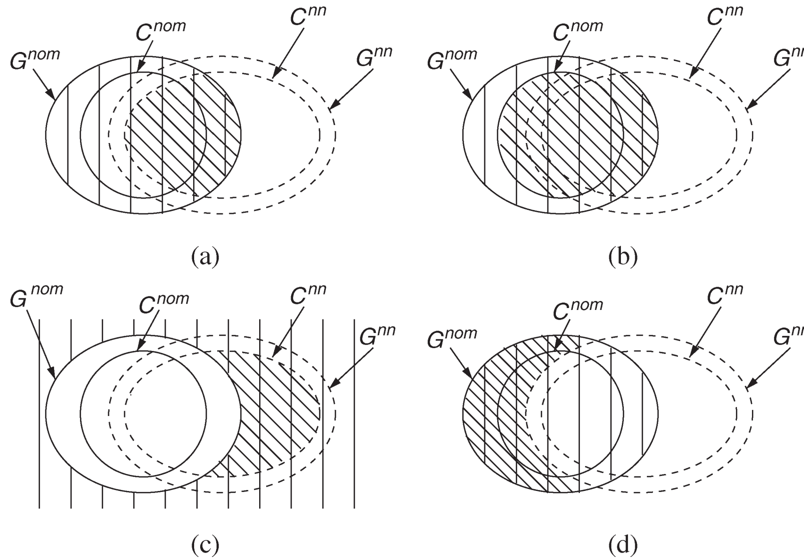


Fig. 3. Venn diagram for (a) nonnominal fault coverage $\mathrm{FC}^{\mathrm{nn}}$ (2), (b) combined fault coverage $\mathrm{FC}^{\mathrm{nn}}_{\mathrm{comb}}$ (3), (c) flaw coverage $\mathrm{FC}^{\mathrm{nn}}_{\mathrm{flaw}}$ (4), and (d) coverage loss $\mathrm{FC}^{\mathrm{nn}}_{\mathrm{loss}}$ [(8), introduced in Section IV]. Diagonal lines indicate the nominator; vertical lines show the denominator.

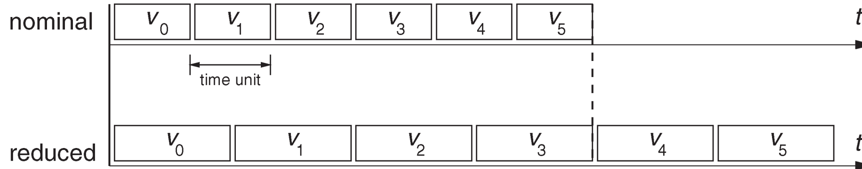


Fig. 4. Performance degradation.

For instance, if C^{nom} is [0 Ω, 800 Ω], G^{nom} is [0 Ω, 1000 Ω], and we lower the temperature or voltage, the intervals may become $C^{\mathrm{nn}} = [0\ \Omega, 1250\ \Omega]$ and $G^{\mathrm{nn}} = [0\ \Omega, 1400\ \Omega]$. Then, the interval in the nominator will be [1000 Ω, 1250 Ω] (all defects cannot be detected by the nominal testing but can be detected by the nonnominal testing), and the interval in the denominator will be [1000 Ω, ∞]. It is obvious that the definition is only sound if there is a limit R_{lim} such that $\rho(r) = 0$ for any $r > R_{\mathrm{lim}}$. This limit can be safely assumed for short defects as ρ is a monotonic decreasing function [20] and the size distribution of particles that cause the short defects is also decreasing [22].

All fault coverages are defined with respect to one fault; for a fault list, average numbers are taken. Fig. 3 shows the definitions in a form of Venn diagrams.

C. Impact of Performance Degradation

Low-voltage testing imposes some performance degradation. This means that the frequency with which the device operates decreases, leading to an increased test application time. If the test-application time is limited, one may be confronted with a choice whether to apply a given test set TS "as it is" at its nominal power supply voltage or to reduce V_{DD} and frequency and to apply a subset $TS' \subsetneq TS$ that requires the same test-application time. Fig. 4 shows the application of six vectors, i.e., $v_0 - v_5$. If the voltage is reduced, individual vectors may detect more defects, but if test-application-time increase is unacceptable, as in Scenario **CN**, only four vectors out of six can be applied. The analysis in this paper allows one to decide which option leads to a better defect coverage.

To further illustrate the tradeoff between the improved detection by vectors and the restriction on their number, assume that, for the example used in this paper, $TS = \{\text{"00"}, \text{"10"}\}$ and $TS' = \{\text{"00"}\}$, where TS' is obtained from TS by truncating its second test vector. The decision problem is whether to apply the test under nominal voltage (and to keep vector "10" which is more efficient than "00" in the test set) or to lower the voltage and, hence, also the frequency.[3] In the electrical situation previously proposed, reducing the voltage results in detecting all defects detectable by the vector "10" and even some additional flaws. Hence, in our example, this option is superior. However, if $R^{\mathrm{nn}}_{00} < R^{\mathrm{nom}}_{10}$ would hold, leaving "10" in TS would appear to be the better choice than lowering the power supply voltage.

In order to accurately determine the benefit of low-voltage testing, given a test-application-time budget, we define a time unit as the duration of a clock cycle for the nominal frequency. For testing under nominal conditions, k test vectors can be applied to the circuit in k time units. Let the performance degradation necessitated by low-voltage testing be expressed by the factor τ_{pd}. Then, the number of vectors that can be applied during the same period of time becomes $\lfloor k/\tau_{\mathrm{pd}} \rfloor$. Coverage

[3] In this simple example and considering only the mentioned short defect, it would be more efficient to exclude from TS the vector "00" rather than "10." For a nontrivial circuit, however, excluding the vectors suboptimal for a given resistive short from the test set TS could result in losing coverage of other defects for which they have been generated.

FC (1) of the original test set $TS = \{t_1, t_2, \ldots, t_m\}$ is compared with the nonnominal metric $\mathrm{FC}^{\mathrm{nn}}$ (2) of the pruned test set $TS' = \{t_1, t_2, \ldots, t_{m'}\}$, where $m' = \lfloor m/\tau_{\mathrm{pd}} \rfloor$. Comparing FC and $\mathrm{FC}^{\mathrm{nn}}$ gives the answer whether testing under nominal conditions or low-voltage testing detects more defects within an identical period of time and, thus, is more effective under the test-time constraint imposed by Scenario **CN**.

D. Voltage- and Temperature-Dependence Models

This section describes the modifications in the procedures for calculating C-ADI and G-ADI to obtain the intervals for the nonnominal conditions (C^{nn} and G^{nn}). The procedures consist of two parts: critical resistance computation by local electrical analysis at bridge site (done for C-ADI and G-ADI) and interval propagation (done for C-ADI) or automatic test pattern generation (ATPG, done for G-ADI). Changing the power supply voltage V_{DD} and/or temperature T has implications on the critical resistance calculation but not on the interval propagation or the ATPG procedure.

Critical resistances are calculated analytically using electrical equations. For a gate driven by an n transistor network, the critical resistance is given by

$$R_{\mathrm{crit},n} = \frac{|V_{\mathrm{Tp0}}| - \mathrm{Th} + \sqrt{(V_{\mathrm{DD}} - |V_{\mathrm{Tp0}}|)^2 - \frac{2I_{\mathrm{ds},n}(\mathrm{Th})}{C_{\mathrm{ox}}\mu_{\mathrm{p}}W_{\mathrm{p}}/L_{\mathrm{p}}}}}{I_{\mathrm{ds},n}(\mathrm{Th})} \tag{5}$$

where Th is the logic threshold of the succeeding gate, V_{Tp0}, μ_{p}, W_{p}, and L_{p} are the zero-bias threshold voltage, the mobility, the channel width, and the channel length for a PFET, respectively, and $I_{\mathrm{ds},n}(\mathrm{Th})$ is calculated using

$$I_{\mathrm{ds},n}(V_{\mathrm{ds},n}) = \mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W_{\mathrm{n}}}{L_{\mathrm{n}}} \left((V_{\mathrm{gs},n} - V_{\mathrm{Tn0}})V_{\mathrm{ds},n} - \frac{V_{\mathrm{ds},n}^2}{2} \right) \tag{6}$$

where μ_{n} is the mobility, C_{ox} is the oxide capacity per area unit, and W_{n}, L_{n}, and V_{Tn0} are the channel width, the channel length, and the zero-bias threshold voltage for an NFET, respectively [23], [24]. For a gate driven by the p transistor network, similar equations hold.

Under the nonnominal conditions, R_{crit} shifts to a different value, i.e., $R_{\mathrm{crit}}^{\mathrm{nn}}$ (which may change C-ADI and G-ADI). In addition, the short-defect resistance R_{sh} itself is a function of the temperature.

Dependence of R_{crit} on V_{DD}: V_{DD} is part of (5). Furthermore, the threshold Th of the succeeding gate is a function of voltage. It can be determined using a SPICE simulation or analytically. $R_{\mathrm{crit}}^{\mathrm{nn}}$ is calculated using (5) with new parameters.

Dependence of R_{sh} on T: The impact of temperature change to the resistance of a material is governed by

$$R = R_{\mathrm{ref}} \cdot (1 + \alpha \cdot (T - T_{\mathrm{ref}})) \tag{7}$$

where α is called thermal resistance coefficient, R_{ref} is the resistance at temperature T_{ref}, and T is the actual temperature.

For metals, the resistance rises with increasing temperature. The thermal resistance coefficients α of metals used in semiconductor processing range between 0.003715 and 0.005866 at 293 K.

Dependence of R_{crit} on T: We considered the temperature dependence of the threshold voltage V_{T}, the mobility μ, and the intrinsic carrier concentration n_{i}. We used the temperature-dependence model from the Berkeley Predictive Technology Model (which is provided by the Device Group at UC Berkeley) [25], [26] in connection with the Berkeley Short-Channel IGFET Model 4 (BSIM4). We used BSIM4.4.0 which was released in March 2004 and is available at http://www-device.eecs.berkeley.edu/~bsim3/bsim4.html.

To calculate the critical resistance for low-temperature testing, (5) with new values of V_{T} and μ is employed (and the new value of n_{i} is used for equivalent transistor calculation). Furthermore, the resistance of the defect decreases with the temperature by some factor that can be calculated by (7), taking the thermal resistance coefficients α into account. Suppose that α is 1.2 and that calculated $R_{\mathrm{crit}}^{\mathrm{nn}}$ is 1000 Ω. Then, any short defect with resistance at nominal temperature being less or equal to 1200 Ω will have a resistance of 1000 Ω or less at low temperature, and hence, the faulty effect will be interpreted by the succeeding gate. Consequently, $R_{\mathrm{crit}}^{\mathrm{nn}}$ which is calculated using (5) must be multiplied by the factor of 1.2.

III. Experimental Results

One thousand random test vectors were applied to ISCAS 85 and 89 benchmark circuits. The fault set consisted of 10 000 randomly selected two-line nonfeedback RBFs (representing short defects), where available. austriamicrosystems 0.35-μm technology parameters were used. We employed the density function ρ derived from the one used in [15] for all experiments. We are not aware of more recent published data for resistance distribution of short defects. In an industrial setting, the actual short-defect distribution can be derived from monitor structures manufactured in the same facility or even on the same die as the actual product. The experiments in this paper can be easily repeated using an arbitrary density function. All measurements were performed on a 2-GHz Linux machine with 1-GB RAM using the simulator from [16]. In calculating G-ADI (and, thus, proving which defects are redundant under given conditions), exact SAT-based ATPG procedure from [17] was used.

Our study of resistive feedback faults [27] demonstrated that such faults can alter the circuit's behavior in a highly complex and somewhat unexpected way. For some resistance ranges, they result in oscillation, so that assumptions on the test equipment sensitivity are needed in order to accurately determine the fault coverage. We decided not to introduce another stochastic parameter in our analysis and to concentrate on nonfeedback faults.

A. Scenario *CN*

Scenario **CN** assumes that only low-voltage testing is performed (not complemented by a test run under nominal conditions) and that vectors which exceed the test time spent in

TABLE I
FC^{nn} FOR 10 TIME UNITS

Circ	3.3V	3.0V	2.8V	2.5V	2.0V
c0432	50.89	**51.09**	43.00	41.89	32.68
c0499	61.75	**62.76**	62.26	62.29	51.75
c0880	**81.10**	79.76	80.05	79.71	76.74
c1355	71.79	**73.36**	72.70	72.10	60.25
c1908	**81.47**	81.32	80.01	77.25	69.84
c2670	**68.46**	67.67	67.29	64.79	55.72
c3540	**64.18**	62.16	57.84	53.72	47.06
c5315	69.57	**70.62**	63.09	62.17	56.52
c7552	**75.83**	75.82	73.81	71.44	63.06
cs00208	58.84	**59.72**	56.74	54.92	46.76
cs00298	**86.72**	86.28	85.56	82.94	77.61
cs00344	81.75	**82.19**	79.14	79.40	74.16
cs00349	81.88	**82.23**	79.21	79.47	74.37
cs00382	**83.54**	82.57	82.94	78.95	68.42
cs00386	45.45	46.26	46.56	**46.63**	29.79
cs00400	**82.94**	81.99	82.32	78.58	56.67
cs00420	58.33	**58.55**	57.87	57.16	53.11
cs00444	**61.86**	57.18	57.09	57.46	57.43
cs00510	**74.54**	72.87	72.77	71.44	61.04
cs00526	**73.57**	70.27	70.28	70.96	67.93
cs00641	**90.30**	89.10	88.16	82.98	68.39
cs00713	**89.33**	87.77	86.55	81.37	66.34
cs00820	**39.10**	35.98	34.23	31.44	22.50
cs00832	**37.51**	34.94	34.35	31.24	22.41
cs00838	**53.62**	52.20	52.11	51.08	46.87
cs00953	54.25	55.15	55.30	**55.74**	51.76
cs01196	**41.02**	39.83	39.47	38.27	33.33
cs01238	**42.53**	41.60	41.15	39.89	34.84
cs01423	**71.17**	69.54	69.61	65.36	62.15
cs01488	**45.14**	39.96	39.79	37.17	28.44
cs01494	**44.40**	39.95	39.72	37.12	27.93
cs05378	**75.12**	74.89	72.62	71.47	68.77
cs09234	64.16	**64.44**	63.68	61.47	55.00
cs13207	85.09	**85.84**	85.36	84.52	79.12
cs15850	**76.29**	75.82	75.18	74.17	68.61
cs35932	**69.59**	61.44	61.86	46.95	38.86
cs38417	83.96	**84.94**	84.53	83.10	76.72
cs38584	**67.83**	64.31	64.71	64.72	62.73
Average	66.97	65.85	64.71	62.67	55.15

TABLE II
FC^{nn} FOR 100 TIME UNITS

Circ	3.3V	3.0V	2.8V	2.5V	2.0V
c0432	97.71	98.32	98.43	**98.70**	98.02
c0499	**89.26**	86.42	86.57	86.55	84.81
c0880	96.32	97.14	97.77	**97.98**	97.90
c1355	97.02	97.13	**97.27**	97.15	95.14
c1908	95.07	**95.86**	95.55	95.62	93.41
c2670	92.73	93.59	**93.93**	93.22	90.87
c3540	93.40	**93.77**	93.71	92.79	90.13
c5315	99.02	99.33	**99.35**	99.00	97.88
c7552	97.63	98.23	**98.44**	98.22	97.39
cs00208	**94.66**	93.01	93.26	92.50	90.71
cs00298	98.43	**98.83**	98.69	98.81	98.36
cs00344	99.22	99.28	**99.39**	99.36	98.36
cs00349	99.24	99.29	**99.40**	99.36	98.33
cs00382	99.09	99.40	**99.49**	99.35	98.71
cs00386	**74.47**	73.99	74.41	73.91	73.92
cs00400	99.09	**99.40**	99.33	99.31	98.63
cs00420	80.11	80.29	**80.47**	79.93	76.36
cs00444	98.30	98.74	98.77	**98.88**	97.56
cs00510	97.70	97.89	**98.07**	97.78	96.88
cs00526	96.11	**96.88**	96.15	96.64	95.66
cs00641	98.50	99.24	**99.61**	99.51	99.47
cs00713	98.63	99.26	**99.51**	99.36	99.33
cs00820	**79.48**	77.92	77.57	74.09	69.09
cs00832	**78.60**	77.17	76.69	73.33	67.88
cs00838	62.81	**63.36**	62.65	62.84	62.66
cs00953	86.87	87.17	**87.25**	87.11	85.81
cs01196	**82.68**	82.17	82.59	81.58	76.93
cs01238	83.74	83.42	**83.93**	83.25	79.30
cs01423	96.05	96.76	**97.09**	96.73	95.66
cs01488	**84.49**	83.85	83.57	82.12	77.59
cs01494	**84.10**	83.43	82.92	81.56	77.23
cs05378	93.02	93.62	**93.70**	93.54	92.52
cs09234	78.56	79.37	**80.02**	79.58	78.10
cs13207	93.33	94.49	95.06	**95.27**	94.82
cs15850	90.26	91.26	91.67	**91.69**	91.06
cs35932	**99.32**	99.26	98.94	98.68	97.68
cs38417	95.16	96.27	96.89	**97.12**	96.82
cs38584	88.24	88.90	89.12	**89.21**	88.40
Average	91.27	91.41	91.51	91.10	89.46

the nominal case are cut off. Test-application temperature is not lowered and held constantly at 300 K. To obtain the number of vectors to cut off, we determined the performance-degradation factors τ_{pd} for the power supply voltages of 3.0, 2.8, 2.5, and 2.0 V (with the nominal V_{DD} being 3.3 V) by computing individual gate delays under these voltages and performing critical path analysis. The values of τ_{pd} were between 1.08 and 1.11 (i.e., between 8% and 11%) for 3.0 V, between 1.14 and 1.20 for 2.8 V, between 1.27 and 1.39 for 2.5 V, and between 1.66 and 1.91 for 2.0 V.

Tables I–III report the fault coverage after 10, 100, and 1000 time units, respectively. As a reminder, one time unit corresponds to one clock cycle at the device's nominal frequency. Consider the circuit c1355 and 100 time units. For 3.3 V, which is the nominal V_{DD}, 100 test vectors have been applied, resulting in the fault coverage of 97.02 [computed using (1)]. For 3.0 V, the performance-degradation factor τ_{pd} has been determined to be 1.11. Thus, only 90 test vectors out of originally 100 could be applied; however, they achieved 97.13% coverage FC^{nn} (2). Note that the detections of defects not detectable at 3.3 V are not accounted for. Consequently, if only 100 time units are at our disposal, it is better to lower V_{DD} and to apply the first 90 vectors of the test set than to apply all 100 vectors at the nominal V_{DD}. For 2.8, 2.5, and 2.0 V, the values of τ_{pd} are 1.20, 1.38, and 1.91, and the numbers of applied vectors are 83, 72, and 52, respectively. From the fault-coverage figures in Table II, it can be seen that it is maximal for 2.8 V (which is indicated by the bold font).

The results suggest that low-voltage testing under Scenario **CN** pays off better when more test time is available. While for 10 and 100 time units, testing at the nominal V_{DD} is optimal for quite a few circuits, this almost disappears for 1000 time units. In addition, the optimal voltage tends to drop with increasing test-time limit.

Fig. 5 shows the fault coverage FC^{nn} in graph form as a function of test time for different power supply voltages. The first graph covers the first 100 time units, whereas the second one shows time units 100 through 1000. It can be seen that in the beginning of the test, the coverages (adjusted for performance impact) for 2.5, 2.8, and 3.0 V and the nominal voltage are close together. In the second graph, the curve for 2.5 V turns out to be most efficient, whereas the nominal voltage saturates, not achieving the same test quality despite more vectors being applied. Note that the y-axis of the second graph shows coverages between 90% and 100%. The curve for 2.0 V is relatively low in the beginning, but it overtakes the nominal voltage soon after 100 time units. This is consistent with the conclusions previously drawn.

Table IV shows the flaw coverage (4) for four values of V_{DD} for 1000 time units. The power supply voltage of 2.0 V seems

TABLE III
FC^{nn} FOR 1000 TIME UNITS

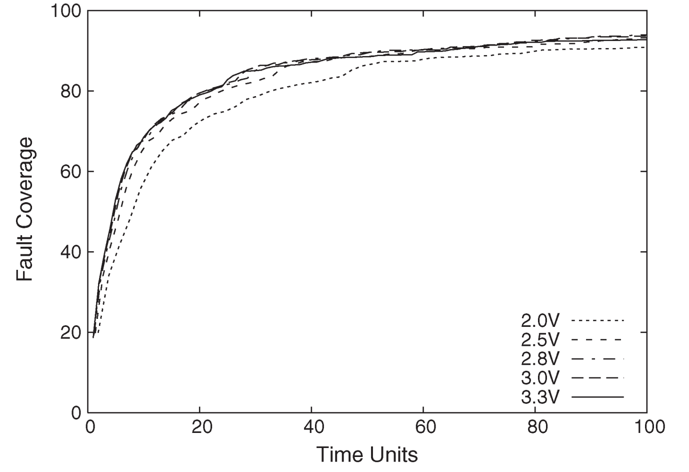
Circ	3.3V	3.0V	2.8V	2.5V	2.0V
c0432	99.78	99.90	99.96	**100.00**	99.94
c0499	99.99	100.00	**100.00**	**100.00**	99.95
c0880	98.88	99.26	99.47	99.74	**99.90**
c1355	99.89	**99.93**	99.92	99.90	99.80
c1908	99.25	99.52	**99.53**	99.46	99.37
c2670	95.93	96.62	96.90	**96.97**	96.84
c3540	99.19	**99.43**	99.41	99.41	99.11
c5315	99.96	99.99	100.00	**100.00**	**100.00**
c7552	99.12	99.46	99.57	**99.60**	99.59
cs00208	**99.56**	99.52	99.53	99.33	98.25
cs00298	99.98	99.99	99.99	100.00	**100.00**
cs00344	99.97	99.98	99.98	99.99	**100.00**
cs00349	99.97	99.98	99.98	99.99	**100.00**
cs00382	99.96	99.97	99.98	99.98	**99.99**
cs00386	**99.82**	99.46	99.46	99.49	98.95
cs00400	99.96	99.98	99.98	99.98	**99.99**
cs00420	85.20	85.63	85.82	**86.02**	85.96
cs00444	99.98	99.98	**99.99**	99.96	99.96
cs00510	99.98	99.99	99.99	**99.99**	99.85
cs00526	99.44	99.62	99.73	**99.80**	99.59
cs00641	99.61	99.84	**99.96**	99.92	99.92
cs00713	99.68	99.84	**99.93**	99.90	99.90
cs00820	96.29	96.49	96.60	**96.64**	95.99
cs00832	96.13	96.31	96.44	**96.47**	95.69
cs00838	69.83	70.29	70.53	**70.76**	70.27
cs00953	97.33	97.76	98.00	**98.19**	98.13
cs01196	96.07	96.57	**96.78**	96.71	95.92
cs01238	96.49	96.96	97.12	**97.24**	96.71
cs01423	99.21	99.49	99.65	**99.80**	99.75
cs01488	99.65	99.77	**99.81**	99.77	99.47
cs01494	99.66	99.77	**99.82**	99.71	99.51
cs05378	98.68	98.91	99.04	**99.16**	99.00
cs09234	90.92	91.37	**91.61**	91.23	89.06
cs13207	95.90	96.86	97.17	**97.26**	97.09
cs15850	96.76	97.39	97.40	**97.52**	97.20
cs35932	**100.00**	**100.00**	**100.00**	**100.00**	**100.00**
cs38417	97.73	98.48	98.77	**98.94**	98.87
cs38584	92.42	92.77	92.95	**93.06**	92.43
Average	97.32	97.55	97.65	97.68	97.42

to be a good voltage to detect flaws—although the number of vectors actually applied is low. However, this is paid by suboptimal coverage. It seems that, if only one test run can be afforded, low-voltage testing is efficient, but the voltage should be lowered moderately, i.e., 2.5, 2.8, or 3.0 V, rather than to the lowest considered value of 2.0 V.

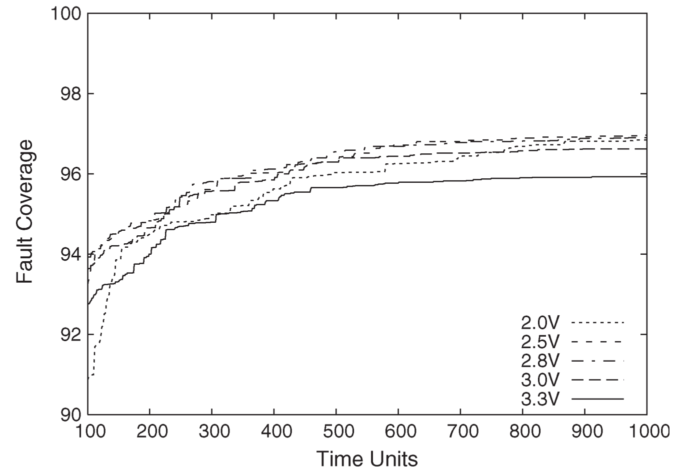
B. Scenario AS

Scenario **AS** assumes a test run under the nonnominal conditions in addition to one under the nominal conditions. Low-temperature testing is allowed in addition to low-voltage testing, and no performance degradation is accounted for as the complete test set is always applied.

We performed experiments for two values of T^{nom}: 300 K and 370 K. During testing, the device dissipates power which leads to increased junction temperature, unless the temperature is controlled during (nominal) testing using a thermal chuck. T^{nom} of 300 K is valid when the temperature is controlled, whereas T^{nom} of 370 K holds if the temperature is not controlled. Note that the packaged IC operates under temperatures closer to 370 K than to 300 K. We considered the V_{DD} values of 3.0, 2.8, 2.5, and 2.0 V and the temperatures of 300 K and 196 K (which is the evaporating temperature of nitrogen) as the nonnominal conditions. In [7], 373 K (100 °C) was taken as the nominal temperature and 273 K (0 °C) as low temperature.



(a)



(b)

Fig. 5. FC^{nn} for c2670 and different V_{DD}'s as a function of test time for time units (a) 0–100 and (b) 100–1000.

We chose a higher value of 300 K for our "low-temperature" scenario, as it is less likely to lead to condensation issues.

We took the values of the constants required for the temperature-dependence model from the same SPICE technology card that was used to derive all other parameters. We assumed that the defect material is aluminum, which resulted in a resistance reduction by a factor of 1.29292 between the nominal and low temperatures for $T^{\mathrm{nom}} = 370$ K and $T = 300$ K.

Table V reports FC^{nn}_{comb} for $T^{\mathrm{nom}} = 370$ K and $T = 300$ K. It quotes the RBF coverage at the nominal temperature and voltage (1) followed by the combined fault coverage obtained after applying the same vectors at the nominal and lower temperatures and a different voltage. (3). The numbers in column 3 are obtained by lowering only the temperature, whereas the numbers in columns 4–7 result from simultaneously lowering the voltage and the temperature.

It can be seen that the fault coverage does increase, but the increase is not very large (less than 1% on average). We performed the same experiment for different values of T and T^{nom}. The average results are reported in Table VI (note that the last row of the table describes testing at the nominal temperature). We can conclude that the increase in the coverage of

TABLE IV
FC^{nn}_{flaw} FOR 1000 TIME UNITS

Circ	1000 time units			
	3.0V	2.8V	2.5V	2.0V
c0432	23.47	39.39	60.22	**88.62**
c0499	18.73	33.61	53.40	**85.82**
c0880	21.34	35.29	55.65	**87.18**
c1355	17.64	31.92	51.53	**85.28**
c1908	18.87	33.09	52.65	**84.09**
c2670	17.28	30.75	51.46	**83.95**
c3540	20.97	35.46	56.28	**86.99**
c5315	20.34	34.97	56.45	**88.18**
c7552	19.02	33.34	54.50	**86.93**
cs00208	22.80	37.32	58.67	**86.65**
cs00298	23.26	38.12	60.00	**89.28**
cs00344	22.00	36.00	57.65	**88.15**
cs00349	22.07	36.13	57.80	**88.25**
cs00382	24.82	40.32	62.43	**90.44**
cs00386	20.73	34.40	55.84	**86.76**
cs00400	24.65	40.11	62.12	**90.26**
cs00420	17.86	29.70	47.92	**74.25**
cs00444	23.59	38.97	60.19	**89.25**
cs00510	24.56	40.05	61.82	**89.91**
cs00526	23.87	38.64	60.08	**88.40**
cs00641	20.64	35.05	55.78	**88.20**
cs00713	20.74	35.18	55.85	**88.03**
cs00820	23.24	37.95	57.98	**84.02**
cs00832	23.33	38.08	58.10	**83.93**
cs00838	14.09	23.55	38.21	**59.47**
cs00953	21.48	35.73	56.85	**86.31**
cs01196	19.38	32.79	53.52	**83.08**
cs01238	19.54	33.13	53.99	**83.62**
cs01423	21.18	35.31	56.20	**87.43**
cs01488	21.38	35.25	57.27	**88.09**
cs01494	21.39	35.26	57.26	**88.18**
cs05378	25.67	40.78	62.80	**90.42**
cs09234	16.27	28.00	46.90	**76.97**
cs13207	17.86	30.68	51.04	**84.77**
cs15850	18.98	31.99	52.35	**85.08**
cs35932	19.46	33.51	53.73	**85.84**
cs38417	19.15	32.63	53.73	**86.73**
cs38584	19.12	32.01	51.57	**80.22**
Average	20.81	34.85	55.52	85.50

TABLE V
COMBINED FAULT COVERAGE FC^{nn}_{comb} FOR $T^{nom} = 370$ K, $T = 300$, $V^{nom}_{DD} = 3.3$ V, AND DIFFERENT VALUES OF V_{DD}

Circ	FC	FC^{nn}_{comb}				
		3.3V	3.0V	2.8V	2.5V	2.0V
c0432	99.84	99.88	99.91	99.94	99.98	100.00
c0499	99.99	100.00	100.00	100.00	100.00	100.00
c0880	98.52	99.10	99.33	99.51	99.74	99.91
c1355	99.90	99.94	99.96	99.97	99.99	100.00
c1908	99.08	99.33	99.43	99.51	99.60	99.69
c2670	92.96	93.88	94.14	94.22	94.39	94.62
c3540	99.25	99.47	99.54	99.57	99.62	99.66
c5315	99.88	99.93	99.96	99.98	99.99	100.00
c7552	97.99	98.39	98.50	98.55	98.64	98.76
cs00208	99.57	99.73	99.78	99.80	99.81	99.82
cs00298	99.99	100.00	100.00	100.00	100.00	100.00
cs00344	99.97	99.99	99.99	99.99	100.00	100.00
cs00349	99.97	99.99	99.99	99.99	100.00	100.00
cs00382	99.96	99.97	99.98	99.98	99.99	99.99
cs00386	99.78	99.90	99.93	99.93	99.94	99.94
cs00400	99.96	99.97	99.98	99.98	99.99	99.99
cs00420	83.84	84.68	84.97	85.09	85.26	85.41
cs00444	99.99	99.99	100.00	100.00	100.00	100.00
cs00510	99.97	99.98	99.99	99.99	99.99	100.00
cs00526	99.56	99.70	99.79	99.82	99.85	99.88
cs00641	99.56	99.86	99.91	99.94	99.97	99.97
cs00713	99.61	99.86	99.91	99.93	99.95	99.95
cs00820	95.88	96.36	96.66	96.74	96.85	96.97
cs00832	95.48	95.92	96.21	96.30	96.41	96.54
cs00838	68.10	68.79	69.02	69.14	69.36	69.59
cs00953	97.24	97.65	97.84	97.95	98.09	98.20
cs01196	95.17	96.14	96.50	96.66	96.83	97.00
cs01238	95.29	96.19	96.56	96.72	96.92	97.12
cs01423	98.92	99.42	99.59	99.65	99.73	99.77
cs01488	99.62	99.79	99.84	99.85	99.85	99.85
cs01494	99.66	99.80	99.84	99.85	99.85	99.85
cs05378	98.57	99.02	99.24	99.31	99.37	99.39
cs09234	89.77	91.14	91.58	91.75	91.92	92.05
cs13207	94.15	95.34	95.76	95.93	96.11	96.27
cs15850	94.77	95.59	95.90	96.05	96.20	96.32
cs35932	100.00	100.00	100.00	100.00	100.00	100.00
cs38417	95.53	96.39	96.71	96.88	97.06	97.20
cs38584	92.15	92.77	93.02	93.16	93.34	93.51
Average	96.83	97.21	97.35	97.41	97.49	97.56

TABLE VI
AVERAGE FC^{nn}_{comb} FOR DIFFERENT V_{DD}'s, T^{nom}'s, AND T's

T^{nom}	T	FC^{nn}_{comb}				
		3.3V	3.0V	2.8V	2.5V	2.0V
300	196	97.35	97.41	97.43	97.44	97.52
370	196	97.46	97.49	97.51	97.52	97.59
370	300	97.21	97.35	97.41	97.49	97.56
370	370	96.83	97.11	97.23	97.40	97.55

detectable defects is limited. Furthermore, the advantage of the combined low-temperature and low-voltage testing over low-voltage testing alone is almost negligible. Given the relatively high cost of low-temperature test, it appears not to be efficient in detecting the hard defects.

In contrast, very high coverage of flaws by the low-X testing in Scenario **AS** is achieved. Tables VII–X summarize the results for the flaw coverage (4). The average numbers are shown in graph form in Fig. 6. It can be seen that the low-voltage and low-temperature testing indeed cover a significant share of flaws. The combination of both techniques is particularly effective, yielding up to 92% of flaws. Low-temperature testing has the largest effect if the voltage cannot be lowered to very small values. For instance, lowering the voltage from 3.3 to 2.5 V yields approximately 60% of the flaws. However, almost the same flaw coverage can be achieved for V_{DD} of just 3.0 V if the temperature is lowered.

C. Discussion

Low-voltage testing is a cost-efficient technique for enhancing the detection capabilities of a test set. It imposes no limits on the test equipment and does not require any additional design for testability logic. Its main cost is the performance degradation such that not all vectors of a test set can be applied due to test-time restrictions. We analyzed whether the defect coverage increase compensates for this effect. It turned out that low-voltage testing is increasingly advantageous when the test set becomes large. Furthermore, we studied the question which voltage level V_{DD} should be lowered to. This value seems to decrease for larger test sets. In contrast, experimental results for low-temperature testing suggest that the coverage increase is limited for the hard defects. In comparing the performance of the combined low-voltage and low-temperature testing and low-voltage testing alone, the relatively high cost of temperature control does not appear to be justified for detecting the hard defects.

The detection of flaws by low-voltage testing is optimal when the voltage is reduced to the lowest meaningful level, whether the performance degradation is accounted for or

TABLE VII
FLAW COVERAGE FC^{nn}_{flaw} for $V^{nom}_{DD} = 3.3$ V, $T^{nom} = T = 370$ K, AND DIFFERENT VALUES OF V_{DD}

Circuit	3.0V	2.8V	2.5V	2.0V
c0432	51.55	68.35	83.41	95.61
c0499	34.90	50.90	68.16	88.70
c0880	33.07	48.06	64.50	84.15
c1355	49.23	69.70	87.21	97.63
c1908	34.56	50.70	67.96	86.28
c2670	28.25	40.77	57.36	79.51
c3540	32.90	46.15	63.71	86.57
c5315	34.85	49.68	67.80	89.63
c7552	34.13	49.93	67.83	87.63
cs00208	27.91	42.60	62.10	86.80
cs00298	26.30	38.19	55.72	83.16
cs00344	25.07	40.15	60.67	86.37
cs00349	25.32	40.38	61.10	86.66
cs00382	37.94	54.10	72.98	92.11
cs00386	18.03	28.57	48.37	80.84
cs00400	38.15	54.48	73.25	92.14
cs00420	21.08	32.15	47.91	70.25
cs00444	40.28	57.76	75.89	93.48
cs00510	29.91	44.63	64.45	89.41
cs00526	27.13	38.50	58.59	84.30
cs00641	18.96	28.75	49.33	80.91
cs00713	19.33	29.66	50.09	81.23
cs00820	27.13	37.41	55.24	79.77
cs00832	27.12	37.06	54.77	79.34
cs00838	16.80	25.54	38.06	56.49
cs00953	28.29	43.18	62.89	85.23
cs01196	28.10	40.60	57.86	81.23
cs01238	29.46	42.08	58.77	81.18
cs01423	25.66	40.09	59.51	84.81
cs01488	23.23	35.34	54.93	84.21
cs01494	23.53	35.66	55.18	84.34
cs05378	32.85	46.65	66.27	88.88
cs09234	18.76	28.87	46.54	73.02
cs13207	20.71	31.46	50.30	77.14
cs15850	21.58	33.12	52.30	78.75
cs35932	36.49	53.72	71.81	87.32
cs38417	22.63	34.88	53.67	79.61
cs38584	23.63	36.25	53.34	76.40
Average	28.81	42.27	60.52	83.71

TABLE VIII
FLAW COVERAGE FC^{nn}_{flaw} FOR $V^{nom}_{DD} = 3.3$ V, $T^{nom} = 370$ K, $T = 300$ K, AND DIFFERENT VALUES OF V_{DD}

Circuit	3.3V	3.0V	2.8V	2.5V	2.0V
c0432	5.94	33.24	54.55	80.78	97.17
c0499	11.50	13.51	32.71	68.63	94.73
c0880	14.90	32.43	50.35	72.64	92.72
c1355	1.63	11.13	37.46	76.03	97.44
c1908	12.34	23.19	43.51	71.38	92.03
c2670	17.37	30.29	45.50	67.77	87.16
c3540	23.69	41.16	55.87	76.29	94.88
c5315	20.78	34.16	51.14	76.27	96.43
c7552	15.66	28.16	46.79	73.42	93.45
cs00208	23.99	42.36	57.33	76.83	95.18
cs00298	24.08	40.57	54.20	74.24	94.87
cs00344	26.16	43.30	57.27	76.66	95.38
cs00349	25.69	42.84	56.92	76.55	95.50
cs00382	18.12	39.17	55.50	78.37	96.91
cs00386	30.36	44.03	55.72	73.25	94.29
cs00400	16.69	37.19	54.50	77.75	96.76
cs00420	18.52	33.71	45.74	61.82	79.00
cs00444	12.78	29.39	49.44	77.20	96.78
cs00510	17.51	34.65	52.21	75.38	96.04
cs00526	21.06	39.46	52.12	73.56	93.70
cs00641	31.13	46.83	58.50	74.76	95.36
cs00713	30.62	45.83	57.91	74.66	95.18
cs00820	16.93	36.82	48.26	67.34	87.94
cs00832	16.44	35.98	47.32	66.60	87.54
cs00838	14.41	26.50	36.11	48.99	62.81
cs00953	14.91	30.52	47.38	69.94	92.14
cs01196	16.93	33.28	48.67	69.50	89.70
cs01238	16.04	33.09	48.72	69.44	89.16
cs01423	22.57	40.86	55.43	74.74	94.68
cs01488	31.26	49.67	60.58	76.79	95.49
cs01494	31.40	49.87	60.79	76.93	95.54
cs05378	23.79	52.74	64.75	80.59	96.41
cs09234	21.17	34.71	46.69	64.60	84.76
cs13207	22.07	35.75	48.64	68.00	89.10
cs15850	23.91	38.68	51.29	70.09	90.18
cs35932	9.82	18.20	37.53	68.96	89.82
cs38417	23.60	39.83	52.43	70.89	90.68
cs38584	20.42	36.78	49.40	67.28	85.71
Average	19.67	35.79	50.77	72.23	91.91

not. The coverage of flaws is significantly improved by low-temperature testing. This renders the combined low-voltage and low-temperature testing the method of choice to detect dynamic and reliability defects by (static) scan test. While low-temperature testing is expensive, the alternatives, such as burn-in, are also associated with high extra costs.

If no test cost increase is acceptable, the low-X testing is restricted to low-voltage testing, and the test set must be stripped. In this case, testing at slightly reduced voltage improves the detection of hard defects while detecting a significant number of flaws. However, testing at a very-low voltage does not yield the optimal coverage and, thus, seems to be advisable only in addition to a second test application at the nominal V_{DD} and T. The same holds in the case of low-temperature testing. Testing under both the nominal and nonnominal conditions results in a large improvement in coverage of the hard defects and is very efficient in detecting flaws, particularly for very low values of V_{DD} and T.

IV. COVERAGE LOSS BY LOW-VOLTAGE TESTING

Conventional wisdom states that lowering the power supply voltage extends the resistance range in which the short defect is detectable. Somewhat surprisingly, we demonstrate that a short defect with a certain resistance which has been detected at the nominal V_{DD} becomes undetectable by low-voltage testing.

Consider the circuit in Fig. 7. Its single input a is inverted, and the output of the inverter b has a resistive stuck-at-zero fault. The voltage characteristics on line b for the pattern "0" under nominal conditions and the reduced power supply voltage are shown in Fig. 8 (as V^{nom} and V^{nn}). The AND gate C and the OR gate D succeed the short defect; their side inputs are fixed to noncontrolling values. The thresholds of C and D are not equal; they are shown in Fig. 8 as Th^{nom}_C and Th^{nom}_D, respectively, when the power supply voltage is a nominal voltage, and Th^{nn}_C and Th^{nn}_D, respectively, for low-voltage testing.

The analysis of detectability for the nominal voltage is similar to [13]. The good values at the lines c, d, and e are one, one, and zero, respectively. Let the critical resistances for the inputs of the gates C and D be R^{nom}_C and R^{nom}_D, respectively. For $R_{sh} < R^{nom}_C$, the gate C interprets the logical value of zero at its inputs and drives a zero at its output c. Similarly, D drives zero at d, and the logical value at the output e is zero (no detection). For $R^{nom}_C < R_{sh} < R^{nom}_D$, however, the logical values at c, d, and e are one, zero, and one, respectively, which means that the fault is detected. For $R_{sh} > R^{nom}_D$, the behavior is identical to the fault-free case (no detection).

TABLE IX
FLAW COVERAGE FC_{flaw}^{nn} FOR $V_{DD}^{nom} = 3.3$ V, $T^{nom} = 370$ K, $T = 196$ K, AND DIFFERENT VALUES OF V_{DD}

Circuit	3.3V	3.0V	2.8V	2.5V	2.0V
c0432	24.34	29.69	43.50	70.35	90.49
c0499	28.52	30.97	38.62	48.64	72.38
c0880	40.70	47.98	56.21	77.17	97.61
c1355	4.63	5.65	8.73	29.53	54.52
c1908	29.92	34.91	42.55	60.52	92.21
c2670	45.01	52.07	58.78	70.67	88.97
c3540	57.53	65.30	71.74	81.54	96.92
c5315	49.55	56.43	63.76	76.90	98.68
c7552	39.35	45.47	53.36	69.26	94.79
cs00208	63.06	72.78	78.24	87.01	95.78
cs00298	64.11	70.76	76.89	90.34	98.96
cs00344	66.65	75.78	80.46	86.59	97.32
cs00349	66.37	75.65	80.64	86.99	97.13
cs00382	49.31	57.99	64.22	79.00	96.63
cs00386	76.28	84.32	89.96	95.65	98.69
cs00400	46.79	55.24	61.89	78.05	95.93
cs00420	51.60	60.62	65.73	73.34	81.59
cs00444	35.64	42.40	48.82	63.13	90.18
cs00510	51.74	60.30	68.27	82.87	95.30
cs00526	58.93	67.45	73.18	84.28	96.57
cs00641	75.30	84.15	90.28	96.30	99.68
cs00713	73.98	82.59	88.50	94.30	99.34
cs00820	49.10	57.81	63.94	77.45	89.93
cs00832	47.81	56.53	62.75	76.39	89.73
cs00838	40.41	47.49	51.53	57.58	64.42
cs00953	44.30	54.01	60.74	73.83	86.08
cs01196	47.76	56.13	62.86	77.20	92.60
cs01238	45.91	54.24	61.08	76.04	91.68
cs01423	60.18	70.63	78.91	89.77	96.99
cs01488	77.00	86.58	91.55	96.68	99.35
cs01494	77.10	86.68	91.61	96.71	99.37
cs05378	68.01	84.50	90.60	96.50	99.24
cs09234	55.07	63.71	69.82	77.38	88.96
cs13207	56.27	64.98	72.09	80.25	93.60
cs15850	59.09	68.03	74.69	82.55	94.13
cs35932	23.83	27.55	33.42	46.37	73.08
cs38417	59.93	69.57	75.51	82.85	95.32
cs38584	53.29	62.25	68.62	77.96	88.00
Average	51.69	59.72	66.16	77.58	91.37

TABLE X
FLAW COVERAGE FC_{flaw}^{nn} FOR $V_{DD}^{nom} = 3.3$ V, $T^{nom} = 300$ K, $T = 196$ K, AND DIFFERENT VALUES OF V_{DD}

Circuit	3.3V	3.0V	2.8V	2.5V	2.0V
c0432	21.50	30.66	46.20	72.66	90.24
c0499	22.59	29.52	36.87	54.63	71.93
c0880	31.13	42.51	54.23	79.06	97.37
c1355	4.33	7.19	10.89	36.12	54.06
c1908	23.33	33.50	41.74	68.53	91.94
c2670	33.47	46.14	54.73	72.75	88.49
c3540	43.69	57.46	65.87	82.24	96.50
c5315	37.88	51.18	59.91	80.33	98.16
c7552	30.33	42.53	51.17	74.34	94.23
cs00208	47.10	61.39	70.19	84.68	95.42
cs00298	48.42	59.05	69.43	87.15	98.75
cs00344	50.02	63.48	71.38	84.70	96.93
cs00349	49.98	63.72	71.86	84.93	96.74
cs00382	37.77	52.51	62.48	81.63	96.25
cs00386	56.83	69.53	78.81	89.86	98.29
cs00400	36.15	50.78	60.98	80.75	95.54
cs00420	37.83	50.49	58.32	71.09	81.26
cs00444	27.87	38.98	47.07	69.95	89.75
cs00510	40.00	52.32	63.47	81.55	95.01
cs00526	44.59	57.07	66.40	82.32	96.78
cs00641	55.36	69.85	79.40	90.45	99.24
cs00713	54.47	68.51	77.81	89.24	98.90
cs00820	37.18	48.83	59.44	75.50	90.11
cs00832	36.29	47.77	58.39	74.73	90.15
cs00838	29.49	39.42	45.66	55.95	64.18
cs00953	33.51	47.14	56.74	72.56	86.34
cs01196	35.63	48.42	58.52	77.41	92.21
cs01238	34.34	46.97	57.17	76.49	91.32
cs01423	45.25	61.47	72.00	86.08	96.62
cs01488	57.14	72.31	80.86	91.23	98.97
cs01494	57.23	72.44	80.94	91.28	99.00
cs05378	49.83	71.74	81.06	91.77	98.94
cs09234	39.64	53.44	61.99	76.06	88.53
cs13207	40.96	55.74	64.59	79.60	93.14
cs15850	43.25	58.00	66.85	81.20	93.69
cs35932	18.92	26.96	32.92	53.41	72.51
cs38417	43.77	58.57	67.34	81.55	94.88
cs38584	39.57	52.94	61.97	76.23	87.64
Average	38.86	51.59	60.68	77.37	91.05

Under low-voltage testing, both the voltage characteristic and the threshold shift down, leading to the new critical resistances R_C^{nn} and R_D^{nn}. Using a reasoning similar to the aforementioned case, it can be seen that the fault is detected for $R_C^{nn} < R_{sh} < R_D^{nn}$. Since $[R_C^{nom}, R_D^{nom}]$ is not included in $[R_C^{nn}, R_D^{nn}]$, a short defect with a resistance from the first interval is detected at the nominal voltage but not detected by the same test vector in low-voltage testing. Note that other defects, which are not detected when testing at the nominal V_{DD}, are detected now. Furthermore, in general, other test vectors might cover this defect. However, this is not possible in the example under consideration: The only other pattern possible, i.e., "1," does not excite the fault. Therefore, a short defect detected at the nominal V_{DD} can even become redundant.

The analysis in [2] shows that for some width/length parameters of a transistor, lowering V_{DD} will result in shrinking ADIs, and it is argued that transistors with such parameters are rarely used in practice. This anomalous behavior is not the reason for the coverage loss described here. In our case, the "local" ADIs ([0, R_C] and [0, R_D]) are actually enlarged (which is consistent with the research published before), and the coverage loss results from the propagation through an XOR gate as the reconvergency point. Hence, this behavior is possible for the conventional transistors.

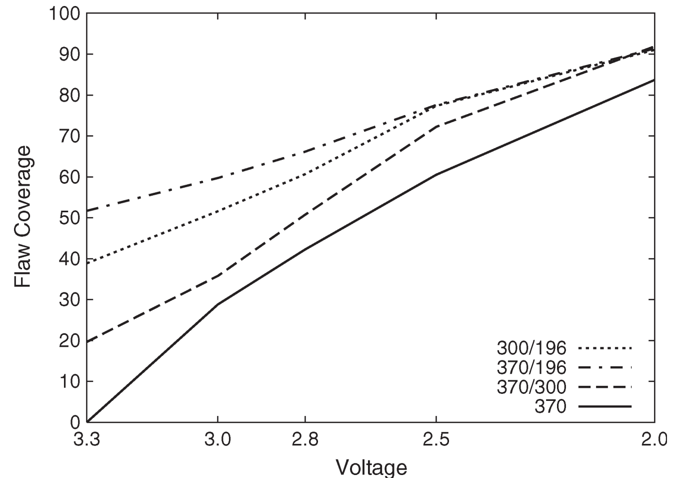


Fig. 6. Average flaw coverage from Tables VII–X.

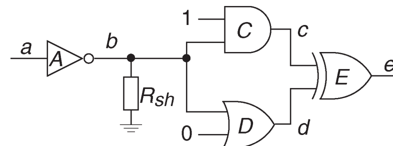


Fig. 7. Example circuit.

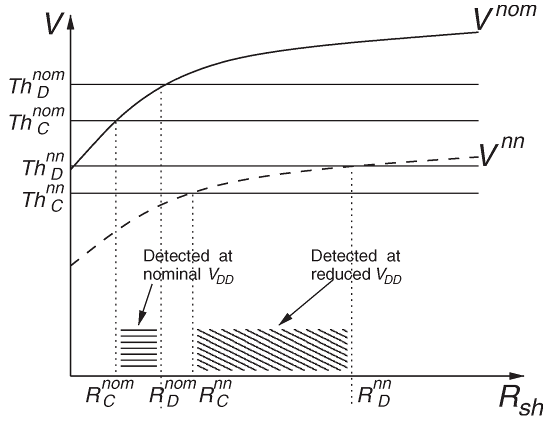


Fig. 8. $R_{\rm sh}-V$ diagram.

TABLE XI
COVERAGE LOSS

Circ	3.0V		2.8V		2.5V		2.0V	
	#F	FC^{nn}_{loss}	#F	FC^{nn}_{loss}	#F	FC^{nn}_{loss}	#F	FC^{nn}_{loss}
c3540	1	0.0003	1	0.0004	1	0.0004	0	0.0000
cs00208	0	0.0000	0	0.0000	0	0.0000	2	0.0222
cs00420	0	0.0000	0	0.0000	0	0.0000	4	0.0176
cs00510	0	0.0000	0	0.0000	0	0.0000	32	0.1404
cs00838	0	0.0000	0	0.0000	0	0.0000	1	0.0044
cs09234	2	0.0125	2	0.0201	2	0.0201	2	0.0201
cs15850	1	0.0003	1	0.0003	1	0.0003	0	0.0000
cs38417	2	0.0009	2	0.0013	0	0.0000	0	0.0000

In order to quantify the coverage loss due to the phenomenon previously described, we introduce the following metric:

$$\mathrm{FC}^{\rm nn}_{\rm loss} = 100\% \cdot \frac{\int_{(G^{\rm nom} \setminus G^{\rm nn})} \rho(r) dr}{\int_{G^{\rm nom}} \rho(r) dr}. \tag{8}$$

Fig. 3(d) shows the definition.

Table XI contains the number of faults for which $G^{\rm nom} \setminus G^{\rm nn}$ is nonempty, i.e., which have resistance ranges that are detectable at nominal voltage but not detectable at low voltage, in the columns marked "#F," and the coverage loss according to (8). Circuits with no such faults are not shown. It can be seen that the coverage loss does occur in practice but its extent is very limited.

V. CONCLUSION

We investigated the effectiveness of the low-X testing, i.e., low-voltage testing, low-temperature testing, and their combinations, in detecting the resistive bridging defects. We enhanced the RBF model in order to account for changes in both the transistor parameters and the particle resistance. We extended the fault-coverage definition for the low-temperature and low-voltage testing, accurately distinguishing between the hard defects that are detectable under nominal conditions and the flaws that are undetectable under nominal conditions. We derived recommendations on the optimal use of the individual techniques and their combinations. Moreover, we demonstrated that in certain situations, low-voltage testing can introduce coverage loss and that such situations occasionally occur for actual benchmark circuits.

Open questions include the implications of lowering $V_{\rm DD}$ on other classes of defects such as resistive opens [5] and its relation to $I_{\rm DDQ}$ testing [28] and outlier screening [29]. Experiments with deterministic rather than random test vectors may yield new information. Extension of the model used here to dynamic behavior (in a way similar to [30]) would allow us to determine the influence of delay defect detection on the coverage for different power supply voltages. Silicon experiments would provide the ultimate proof of the efficiency of the studied methods. Finally, the introduced techniques may be useful for finding optimal test strategies for devices which have to operate under a variety of voltages and temperatures such as dynamic-voltage-scaling circuits.

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