A Specific ATPG technique for Resistive Open with Sequence Recursive Dependency

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Abstract

This paper analyzes the electrical behaviour of resistive opens as a function of their unpredictable resistance. It is demonstrated that the electrical behaviour depends on the value of the open resistance. It is also shown that detection of the open by a given vector T_i recursively depends on all the vectors that have been applied to the circuit before T_i. An electrical analysis of this recursive effect is presented and a specific ATPG strategy is proposed.

1. Introduction

The advent of integrated circuit technology has introduced electronics in many aspects of present-day life. As the use of electronic components increases, the expectation of lower cost, better accuracy and higher reliability increases. Lower cost and better accuracy are achieved by putting more transistors per unit of silicon, using design automation, increasing device operation speed and reducing its power consumption. However, these design steps cannot guarantee reliability. In fact, as the circuit density increases, the probability of a manufacturing defect increases. A higher expectation of reliability can only be met by more thorough and comprehensive testing.

Due to the complexity of IC technological process, many physical defects occur during the manufacturing of any system. The typical defects encountered in today technologies and modeled in yield simulators are the so-called spot defects that may cause shorts and/or opens at one or more of the different conductive levels of the devices. Test generation for any type of defect is obviously not feasible due to the huge amount of CPU time and memory size required. Instead, test generation relies on fault models that are supposed to both represent the defect behavior and allow easy generation of test vectors through ATPG and fault simulation.

Classical fault models (stuck-at, stuck-open, stuck-on, etc.) have been proved to be efficient in the context of ATPG and fault simulation. However, it is well-known that these fault models cover only partially the spectrum of real failures in today's integrated circuits. The increasing demand of low PPM (part per million) defect rates requires the derivation of ever more accurate fault models. In particular, a special attention must be paid to defects that exhibit complex behavior not accurately represented by classical fault models and defects with a high probability of occurrence [1-5]. In modern nanometer process, resistive opens belong to both categories since they change the electrical behavior of the connection and they are predominant defects in today technologies in which copper is used for interconnections.

A number of research works have been conducted in the past years dealing with the electrical characterization and modeling of this kind of failure [6-9]. Classically, it is considered that the connection is fully open, i.e. the following gates are completely disconnected and called 'floating gates'.

In this paper, we analyze the case where the following gates are still connected but through a degraded line exhibiting some resistance [10-17]. It is important to note that the value of this resistance is an unpredictable parameter of the defect. The electrical behavior of the defect obviously depends on this random parameter as well as its detection conditions. In order to optimize and guarantee the detection of such a defect, its electrical behavior has to be analyzed as a function of this random parameter and optimal detection conditions must be derived.

The paper will be organized as follows. Section 2 presents a very detailed analysis of the electrical behavior of resistive opens. The detection of the open is analyzed considering a sequence of 2 test vectors, then considering a sequence of n test vectors. Starting from this analysis, section 3 proposes a new and specific ATPG for resistive opens. Finally, section 4 gives some concluding remarks.

2. Resistive open behavior and detection

In this section, an electrical analysis of the resistive open is conducted using a didactic circuit. Figure 1 gives an example of an extremely simple circuit where node n_4 is affected by a resistive open. This didactic circuit has 4

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inputs (I_1, I_2, I_3, I_4) and 2 outputs (O_1, O_2). Note that we do not care for the logic function; we just need a simple example to conduct our electrical analysis. Obviously, the demonstrations given below can be extended to real cases.

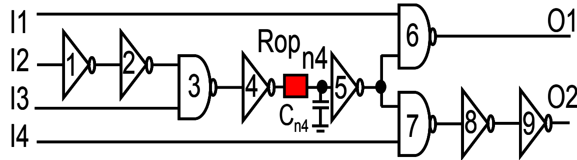

Figure 1: A resistive open

From a static voltage test point of view (Boolean testing), it is well known that a resistive open cannot be detected because the faulty node always ends up reaching its correct logic value. On the contrary, resistive opens modify the timing behavior of the circuit, so they can be detected by a dynamic voltage test strategy (delay testing).

2.1. Detection with a *2*-vector sequence

The open resistance R_{op} is a random parameter of the defect and can not be predicted, but we can simulate different cases of resistance value. In Figure 2, a SPICE simulation of the defective circuit (R_{op} = 3KΩ) using a 180nm technology is first performed. Analysis of the dynamic behavior requires to create some signal transitions on the circuit inputs and to propagate these transitions through the circuit. The initial state is given by vector $T_0 = \langle I_1, I_2, I_3, I_4\rangle = \langle 1010\rangle$ and the transition is created by vector $T_1 = \langle 1110\rangle$. Input I_2 switches from 0 to V_{DD} and the rising edge is propagated to output O_1 through gates 1/2/3/4/5/6.

In this simple example, we consider that we can use a cycle time of about T_{cl} = 0.4ns. The propagation of this rising edge allows to give the following definitions:

- T_{pb} (Propagation Before the defect),
- T_{pa} (Propagation After the defect),
- T_{sl} (Slack Time of path $I2 \rightarrow O1$).

The voltage on node n4 as a function of time is depicted by the solid line. The voltage on node O1 is depicted by the dashed line. Due to the open, it clearly appears that the signal at node n_4 is slowed down. An additional delay T_{op} = 0.13ns appears. But the size of the timing defect is still smaller than the slack time, a correct output value is latched in the output register and the circuit operates correctly. From Figure 2, it is clear that an open with a small resistance (3kΩ) cannot be detected while an open with a large resistance can be detected.

This means that a given resistive open can be detected by the 2-vectors sequence {T_0, T_1} if its unpredictable resistance R_{op} is larger than a critical resistance called $R_c^{\{T0,T1\}}$. In our example, SPICE simulations show that the critical resistance is equal to 7.5kΩ. In other words, we associate to the resistive open the Detection Interval *DI* defined below:

$$DI^{\{T0,T1\}} = [R_c^{\{T0,T1\}}, \infty] = [7.5\text{k}\Omega, \infty] \qquad (1)$$

Note that the above range is associated to the pair of vectors {T_0, T_1}. But in the general case, another pair of vectors may detect even smaller resistances. This could be the case if another propagation path is excited with a smaller slack time.

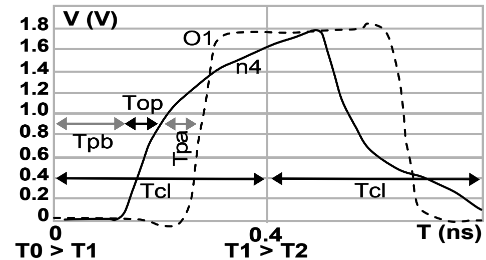

Figure 2: Dynamic behavior

2.2. Detection with an *n*-vector sequence

Now, we consider a more realistic situation where, starting from an initial state given by T_0, a complete test sequence of m vectors is applied to the circuit targeting different defects/faults:

$$\text{Test sequence} = \{T_0, T_1, \ldots, T_{n-1}, T_n, \ldots, T_m\} \qquad (2)$$

In this sequence, we assume now that vector T_n has been specifically generated to detect the resistive open on node n_4. Tn is such that the transitions created by the 2 vectors {T_{n-1}, T_n} are able to detect the resistive open on node n_4. In other words, the pair {T_{n-1}, T_n} creates a transition that passes through node n_4 and is propagated to an observable output.

Table 1: The simulated test sequence

Phase	Vector	Cycle	I_1	I_2	I_3	I_4	Transition Polarity on n_4
	T_0	Initial State	0	0	1	0	
Preparation	T_1	#1	0	1	1	0	+
	T_2	#2	0	0	1	0	-
	T_3	#3	0	1	1	0	+
	T_4	#4	0	1	1	0	stable
	T_5	#5	0	0	1	0	-
Detection	T_6	#6	1	1	1	0	+

It is important to note that the preceding vectors {T_0, T_1, …, T_{n-1}} may create some transitions of node n_4 but these transitions are not propagated to an output, i.e. the

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open is not detected before vector T_n. For detection of the resistive open, we consequently divide the sequence into 2 phases:

- The preparation phase corresponds to the application of the n - 1 vectors $\{T_1, \ldots, T_{n-1}\}$ starting from the initial state T_0, i.e. when the open cannot be detected but the faulty node may switch.
- The detection phase corresponds to the application of vector T_n, i.e. when the faulty node switches and it is observable on the outputs.

As an example, for the resistive open of Figure 1, we consider the preparation phase made of the initial state $\{T_0\}$ and a sequence of 5 vectors $\{T_1, T_2, T_3, T_4, T_5\}$, and the detection phase made of vector $\{T_6\}$, i.e. the case where $n = 6$. These vectors are given in Table 1.

In this simple and didactic example, node n4 is observable on output O_1 only during the 6th cycle when $I_1 = 1$. Vector T_6 has obviously been generated on purpose, i.e. to detect a fault on node n_4 and so it makes node n_4 observable. The previous vectors (T_1, …, T_5) have been generated targeting some other faults.

a) Preparation phase

We first analyze the preparation phase. As commented above, during the first 5 cycles node n_4 is not observable, but it may switch from 0 to 1 or from 1 to 0 according to the activity of the circuit induced by the input vectors. In other words, the successive input vectors may create successive transitions of node n_4. In the fault-free circuit node n_4 switches from Gnd to V_{DD} and vice-versa, but in the faulty circuit the signal is degraded by the resistive open. If the resistance of the open is large enough, the signal is slowed down and it is not always able to reach the V_{DD} and Gnd values as illustrated in Figure 3 with $R_{op} = 7.5\text{k}\Omega$.

Let us explain in detail the example of Figure 3. Input I_2 is initially equal to 0 (initial state T_0) and switches to 1 (T_1) at time t_0. At time $t_0 + T_{pb}$, the rising transition reaches the output of gate 4 and so the voltage $V(t)$ of node n_4 starts switching from $V_0 = Gnd$ to V_{DD}.

Due to the resistance R_{op} of the defect, the time required by $V(t)$ to reach V_{DD} is much higher than the cycle time T_{cl}. At the end of the 1st cycle, i.e. at time $(t_0 + T_{cl})$, input I_2 switches from 1 to 0 (T_2) and this new transition reaches node n_4 at time $(t_0 + T_{cl} + T_{pb})$. This new transition interrupts the previous one even if node n_4 has not yet been able to reach V_{DD}. Consequently, we observe that, during the first cycle, node n_4 rises from $V_0 = V(t_0 + T_{pb}) = 0\text{V}$ to $V_1 = V(t_0 + T_{cl} + T_{pb}) = 1.26\text{V}$.

Obviously, we can make the same demonstration for the second cycle where a new transition on node n_4 interrupts the previous one and the voltage on node n_4 falls from $V_1 = V(t_0 + T_{cl} + T_{pb})$ to $V_2 = V(t_0 + 2T_{cl} + T_{pb})$. In a similar way, the voltage rises from $V_2 = V(t_0 + 2T_{cl} + T_{pb})$ to $V_3 = V(t_0 + 3T_{cl} + T_{pb})$ during the third cycle, etc.

So, we globally observe that the voltage on node n_4 does not simply switch between Gnd and V_{DD}. Instead, it rises and falls according to the input vectors and goes through a set of successive intermediate voltages V_0, V_1, V_2, V_3, V_4, V_5.

Important is the fact that these successive voltages are more or less following the clock of the circuit. Indeed, they appear at a period of time T_{pb} after the clock pulse. In Figure 3, we observe that they appear every T_{cl}. But, this is an oversimplified example where the transition propagates from the input I_2 to the defect using the same path whatever the input vector. So, the different points V_1, V_2... appear always after the same period of time T_{pb} after the clock pulse. In the general case, the period may vary from vector to vector but the transitions are always initiated by the circuit inputs that follow the circuit clock. And so the global period will correspond to the circuit clock frequency T_{cl}. For the above reasons, we will say that the successive intermediate voltages exhibit a pseudo-period equals to the circuit clock T_{cl}.

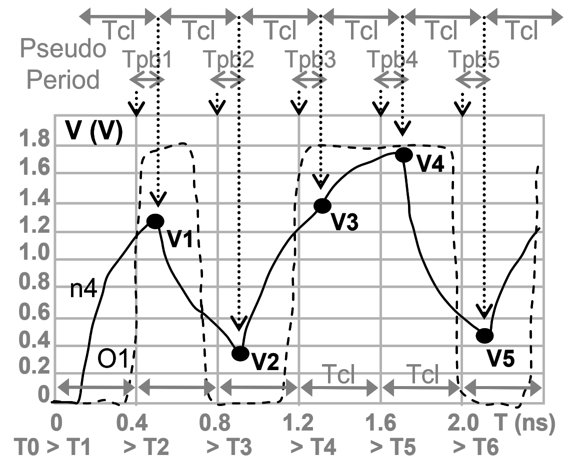

Figure 3: Behavior through a sequence

Very important is also the fact that, for each vector T_j, the corresponding intermediate voltage V_j on node n_i depends on the polarity of the transition, the node electrical parameters R_{ni}, C_{ni}, the strength of the driving gate W^n_i, L^n_i, W^p_i, L^p_i, the defect parameter R_{op}, the pseudo-period T_{cl}, and the previous intermediate voltage V_{j-1}.

In other words, for a given vector T_j, the voltage V_j depends on the resistance of the open and on the previous voltage which **recursively** depends on the resistance of the open and on the previous voltage which in turn depends on the same parameters. Consequently, at the end of the preparation phase, just before the detection phase (vector T_n), the faulty node n_i presents a voltage V_{n-1} which recursively depends on all the previous intermediate voltages, and so it depends on all the previous vectors that have been applied to the circuit.

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b) Detection phase

We now analyze the detection phase using again our small example. When vector T_6 is applied to the circuit, a transition is propagated from input I_2 to node n_4, the transition is delayed by the resistive open, and finally the delayed transition propagates to output O_1.

This situation is quite similar to the one described for the 2-vector sequence in the previous section. An input transition is initiated by 2 vectors: the last vector of the preparation phase T_5 and the vector of the detection phase T_6. So, we come to a similar conclusion: an open with a small resistance can not be detected while an open with a large resistance can be detected.

And so, the resistive open can be detected by the n-vectors sequence $\{T_0, T_1, T_2, T_3, T_4, T_5, T_6\}$ if its unpredictable resistance R_{op} is larger than a critical resistance called $R_c^{\{T0,T1,T2,T3,T4,T5,T6\}}$. Here again, we associate to the resistive open the Detection Interval DI defined below:

$$DI^{\{T0,T1,T2,T3,T4,T5,T6\}} = [R_c^{\{T0,T1,T2,T3,T4,T5,T6\}}, \infty] \quad (3)$$

But there is a fundamental difference between the 2-vector sequence and the n-vector one. In the 2-vector sequence, the additional delay is a function of the initial voltage $V_0 = 0$. While, in the n-vector sequence, the additional delay T_{op} is a function of the previous intermediate voltage V_{n-1}. SPICE simulations show that the critical resistance is equal to $R_c^{\{T0,T1,T2,T3,T4,T5,T6\}} = 28k\Omega$. Note that the above range is completely different from the one obtained in the previous section with the 2-vector sequence $\{T_0, T_1\}$. This clearly demonstrates the significant impact of the preparation phase on the detection of the resistive open.

3. A specific ATPG approach

*I*n this section, the objective is to use the analysis performed in the previous section to derive some guidelines for the development of a specific ATPG tool for resistive opens. Targeting realistic defects, i.e. defects with random parameters, it is clear that the objective of an optimized ATPG should be not only to guarantee defect excitation and propagation, but also to guarantee detection of the defect for the largest possible range of the random parameter, i.e. the smallest possible resistance in our case.

3.1. Specific ATPG strategy

Considering a resistive open on a given node, it has been demonstrated that a given test sequence is able to detect the open for a range of resistance defined by the critical resistance as represented by eq. 12:

$$DI^{\{\text{sequence}\}} = [R_c^{\{\text{sequence}\}}, \infty] \quad (4)$$

The critical resistance is a function of the node electrical parameters (R_{ni}, C_{ni}, W^n_i, L^n_i, W^p_i, L^p_i) and on the slack time T_{sl} during the detection phase. The longer the activated path is, the shorter the slack time is, the smaller the detectable resistance is and the larger the Detection Interval is. This point is quite simple but it has to be considered when a test vector is generated [18].

Principle 1: Considering a given node with a resistive open, the generated test vector should propagate a rising or falling transition through the longest possible path including the faulty node.

Finally, it has also been demonstrated that the critical resistance depends on the final voltage of the preparation phase: V_5. It is clear that the smaller the final voltage is, the smaller the critical resistance is. This means that a minimum critical resistance R_c^{min} could be obtained if the applied test sequence is such that the final voltage of the preparation phase is equal to $V_{n-1} = 0V$.

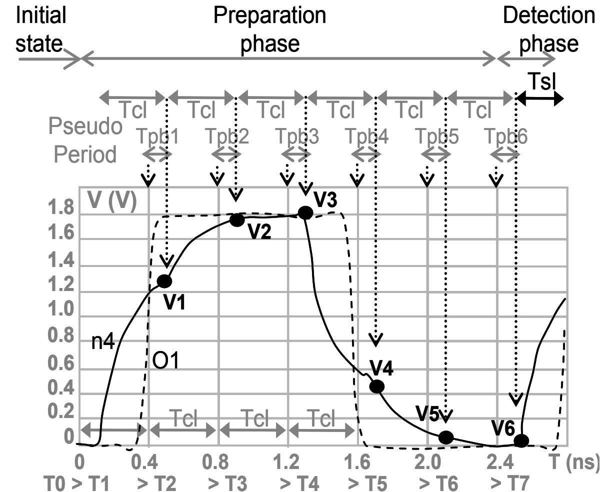

Figure 4: Detection of the minimum resistance

Let us consider Figure 4 giving the SPICE simulation of the circuit of Figure 1 with a new sequence of 7 vectors $\{T_1, T_2, T_3, T_4, T_5, T_6, T_7\}$ where input I_2 successively switches from 0 to 1,1,1,0,0,0 and 1. In this simulation, the resistance of the open is 7.5kΩ. Note that the resistive open in Figure 4 may be considered as detected because the output O_1 switches right after the top of the clock. In fact, it is clear that this resistance is the minimum critical resistance R_c^{min}. In Figure 4, the final voltage V_6 is equal to 0V, which is the best condition to detect the defect with minimum critical resistance. So, Figure 4 illustrates the best case where the detection interval is limited by the minimum detectable resistance.

It is interesting to analyze now how to obtain a final voltage equal to 0V. In Figure 4, the intermediate voltage on node n_4 decreases from V_{DD} to 0V when vectors T_4, T_5

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and T_6 are applied. In fact, these 3 vectors do not create any new transition on node n_4 and so the node has 'enough time' to decrease down to 0V.

From this observation, we conclude that the targeted node n_i can be set to 0V (resp. to V_{DD}) if, before the detection phase, the node remains stable for a given number of consecutive clock cycles. Let us call N^{ni} the required number of consecutive stable cycles (details on how to compute N^{ni} are given in the next section).

So, the basic idea of the proposed ATPG strategy would be to guarantee that, when the detection vector is generated, the targeted node n_i with the resistive open R_{op} has been stable for a given number N^{ni} of consecutive cycles before the switch due to the detection vector. Obviously, a brute force solution consisting in systematically adding N^{ni} vectors before each detection vector is not viable due to the unacceptable increase of the test sequence. Instead, a more efficient solution would be the following:

Principle 2: When ATPG for resistive opens is performed, nodes that have been stable for the required number of consecutive cycles are dynamically targeted.

In other words, the ATPG process could be described through the following points:

- For each node n_i, an activity variable A^{ni} is dynamically computed. This variable indicates the number of consecutive cycles for which the logical value of the node has been equal to its last value.
- A set of candidate nodes is dynamically computed. The candidates are nodes such that $A^{ni} > N^{ni}$.
- A vector T_i is generated for one of the nodes in the set of candidates.

The proposed strategy could be optimal because it does not increase the size of the test sequence and guarantees the coverage of the largest *DI* for each node. Note that the targeted node must not switch for N^{ni} consecutive cycles, not only due to the logic but also due to hazards [19].

3.2. Specific ATPG pre-processing phase

In the above described specific ATPG strategy, a simple solution could be to use the same N ($N^{ni}\ \forall\ n_i$) for every circuit node. In this case a very large overestimation of N would be sufficient to guarantee the final voltage of the nodes. During the ATPG process, when nodes are dynamically targeted, it is also clear that an overestimated N means less candidates. It is not important when ATPG starts with many nodes but it may be a problem at the end of the generation when the whole set of nodes become small. It may be necessary to add vectors to the sequence.

A better solution is to dynamically compute the N^{ni} variable for each defect in the circuit. Indeed, the variable is not fixed and has to be computed for each node, and for each vector. Note that the computation does not need to be extremely accurate, a simple approximation of N^{ni} would be sufficient as long as $N^{ni} < N$.

Figure 5 illustrates the property used to compute N^{ni}. A simple RC model for the node is first assumed where R_c^{min} is the minimum critical resistance and C_{ni} the capacitance of the node. The falling part of the curve corresponds to the preparation phase and the rising part to the detection phase:

- In the rising part, the signal V_{ni} rises from $V_{n\text{-}1}$ = 0V to $V_{DD}/2$ in a period of time equal to T_{sl}. This rising part can be written $$0.5\ .\ \mathrm{Vdd} = \mathrm{Vdd}\ \cdot (1\text{-}e^{-\mathrm{Tsl}/\tau}) \quad (5)$$ where $\tau = R_c^{min} \cdot C_{ni}$

- In the falling part, T_r is the time required for the same node V_{ni} to fall from V_{DD} to 1% V_{DD}. Note that we consider the worst case where $V_{n\text{-}2}$ is equal to V_{DD}. This falling part can be written $$0.01 \cdot \mathrm{Vdd} = \mathrm{Vdd}\ \cdot e^{-\mathrm{Tr}/\tau} \quad (6)$$

From these 2 equations, we deduce that the required time is just proportional to the slack time:

$$T_r = T_{sl} \cdot (\mathrm{Ln}100/\mathrm{Ln}2) \quad (7)$$

$$=> \quad N^{ni} = \mathrm{int}\,[T_r / T_{cl}] \quad (8)$$

The above equation illustrates a very important property: T_r does not depend on R_c^{min} neither on C_{ni}. It only depends on the slack time during the detection phase! The above analysis has been performed assuming a simple RC model and ideal voltage sources. In the realistic case, gates are driving the RC model. So, the relation between the slack time and the required time depends on the driving gate. So, the parameter N^{ni} can be obtained from SPICE simulations for each logic gate.

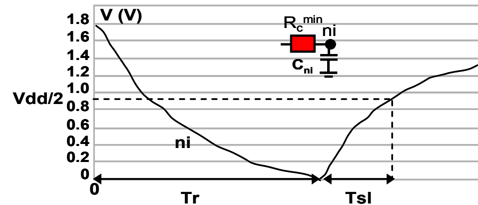

Figure 5: Determination of T_r

But we must keep the ATPG process efficient, and so it is necessary to avoid as much as possible SPICE simulations during the ATPG process. We consequently propose the following strategy based on a pre-processing phase of the gate library.

Assuming that the gate library is available, we perform for each gate a simulation similar to the one illustrated in Figure 5 for an arbitrary capacitance C_{ni}. For different values of the slack time T_{sl} we note the corresponding required time T_r.

For a multi-input NOR or NAND gate, note that the simulations are performed in the worst case conditions,

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i.e. for the most resistive conducting path (only 1 transistor ON for parallel networks).

Such characteristics are illustrated in Figure 6 for an inverter and for a NAND gate. We can observe in Figure 6 that the relation between T_r and T_{sl} is linear and independent of the node capacitance: $T_r = \alpha \cdot T_{sl} + \beta$

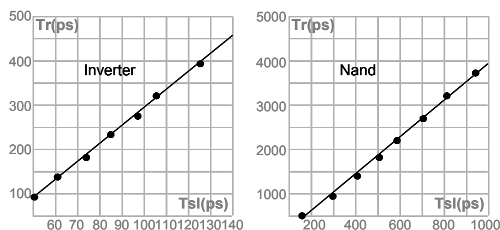

Figure 6: Pre-characterization of T_r vs T_{sl}

Note that the curve obtained in Figure 6 is exact and does not include any approximation to obtain the required time. However, it is possible to add some security margin around T_r by increasing N^{ni} by 1 or 2 clock cycles. Finally, we can now give the proposed ATPG pseudo-algorithm:

- For each remaining node n_i
  - Dynamically compute the activity variable A^{ni}
  - Determine the longest propagation path for n_i
  - Determine the corresponding T_{sl}
  - Determine $T_r = \alpha \cdot T_{sl} + \beta$ (with gate driving n_i)
  - Determine $N^{ni} = T_r / T_{cl}$ (option: $N^{ni} = N^{ni} + 2$)
  - Determine the candidate nodes such that $A^{ni} > N^{ni}$
  - Generate a vector T_n for one of the candidates

4. Conclusion

This paper analyzes the electrical behavior of a resistive open as a function of its unpredictable resistance. It is demonstrated that the detection of the resistive open not only depends on the unpredictable resistance but also on the successive intermediate values of the faulty node, i.e. recursively depends on all the vectors that have been applied to the circuit. An electrical analysis of this recursive effect is presented and a specific ATPG strategy is proposed. The proposed strategy is based on a pre-processing of the gate library. A simple SPICE simulation of each gate in the library with an arbitrary capacitance allow to pre-characterize the gate. The ATPG process does not add additional vectors to the sequence. Instead it dynamically target stable nodes.

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