Resistive Bridge Fault Model Evolution From Conventional to Ultra Deep Submicron Technologies

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Abstract

We present three resistive bridging fault models valid for different CMOS technologies. The models are partitioned into a general framework (which is shared by all three models) and a technology-specific part. The first model is based on Shockley equations and is valid for conventional but not deep submicron CMOS. The second model is obtained by fitting SPICE data. The third resistive bridging fault model uses Berkeley Predictive Technology Model and BSIM4; it is valid for CMOS technologies with feature sizes of 90nm and below, accurately describing non-trivial electrical behavior in that technologies. Experimental results for ISCAS circuits show that the test patterns obtained for the Shockley model are still valid for the Fitted model, but lead to coverage loss under the Predictive model.

Keywords: Resistive bridging faults, Deep submicron technology modeling

1 Introduction

Resistive bridging faults (RBF) are accurate representations of resistive short defects, which are increasingly important for deep submicron and nanoscale CMOS technologies. The first systematic studies on these defects were published in the beginning of the 1990s [1, 2]. Since the bridge resistance is a continuous parameter that is not known in advance, handling of such faults is not a trivial task. Some authors approached the problem by picking a fixed bridge resistance value [3] or by applying a locally exhaustive test set to the bridge site [4].

However, an approach based on *interval algebra* [5, 6] allowed treating the whole continuum of bridge resistance values R_{sh} from zero Ohm to infinity by handling a finite number of discrete intervals. The key observation which enables this efficient method is the following: a resistive short defect changes the voltages on the bridged lines from zero Volt (logic-0) or V_{DD} (logic-1) to some intermediate values; and these intermediate voltages will be different for different R_{sh} values. In order to describe the behavior of a defective circuit, however, it is not necessary to consider the exact voltage on the bridged lines (continuous information). It is rather relevant whether these voltages are *interpreted* as logic-0 or logic-1 by subsequent logic gates (binary, i.e. discrete information). For instance, if a node which is driven to a logic-1 is bridged with a node driven to a logic-0, the voltage on the first node will be close to V_{DD} for very high R_{sh} values and lowest for $R_{sh} = 0\Omega$. A gate fed by that line may interpret a faulty value (logic-0) for $R_{sh} = 0\Omega$ and the correct value (logic-1) for some higher R_{sh} values, depending on the *logic threshold* of the gate. In this case, there is some *critical resistance* value R_{crit}, such that the faulty value is interpreted for $R_{sh} < R_{crit}$ and the correct value is interpreted for $R_{sh} > R_{crit}$. The output of the gate is determined by whether R_{sh} belongs to the interval $[0, R_{crit}]$ or not, rather than on the actual value of R_{sh}.

By propagating the intervals to the outputs, the bridge resistance intervals for which the fault is detected are determined [5, 6]. It has been demonstrated that during this process the intervals may become discontinuous unions of intervals [7]. Non-trivial behavior has been shown for sequential circuits [8] and for feedback faults [9]. Nevertheless, the propagation process is still discrete. The interval arriving on a circuit output is called *analogue detectability interval* (ADI). By calculating the ADI for each output and each applied test vector, the bridge resistance range for which the fault is detected by a test set is determined. This range is called C-ADI (*covered* ADI). It is possible to calculate the *global* ADI (G-ADI), which includes all the bridge resistances for which the fault *could have been* detected. A short defect with $R_{sh} \notin G$-ADI is redundant. A test set can be graded (fault simulated) by relating C-ADI to G-ADI. Several RBF simulators have been proposed [8, 10, 11, 12, 13], some of which employ approximate methods for calculating G-ADI. Also several RBF ATPG tools have been reported [4, 12, 13, 14, 15].

The critical resistance calculation is the only part of the interval-based approach that is technology-dependent. Earlier works employed critical resistance calculation procedure based on Shockley's transistor equations [5, 16, 6, 8] or stor-

ing of the SPICE simulation results in look-up-tables [10]. While Shockley equations (developed in the 1940s) [17] are not necessarily valid for modern deep submicron manufacturing technologies, the look-up-table approach tends to be less flexible.

In this paper we describe the general electrical model (framework) of local circuit behavior at the bridge defect site. It relates the voltage potentials on the bridge nodes to the current flowing through the network. The critical resistance can be calculated as a function of the logic threshold of a succeeding gate. The general framework is based on I-V output characteristics of the PMOSFET and NMOSFET networks and is valid for an arbitrary CMOS technology. It can be instantiated to a *technology-specific model* valid for a given technology by providing actual I-V characteristics.

We demonstrate three instantiations of the general framework. The first model uses Shockley equations and is valid for conventional (not deep submicron) technology (it corresponds to the model used in [5, 6]). The second model is obtained by fitting SPICE data and works well for current CMOS generations. The third model is based on Berkeley Predictive Technology Model (BPTM, which is provided by the Device Group at UC Berkeley) [18] in connection with Berkeley Short-channel IGFET Model 4 (BSIM4),[1] which is valid for 90nm technologies and is used for predicting the transistor behavior in future 65nm and 45nm technologies. BPTM/BSIM4 accounts for the many non-trivial electrical phenomena in these nanoscale technologies, including Non-Uniform Lateral Doping (NULD), Narrow Width Effect, Short-Channel Effect, Drain-Induced Barrier Lowering (DIBL), Drain-Induced Threshold Shift (DITS) and Bulk Charge Effect. Hence, the three models describe past, present and future technologies; nevertheless they share the same basic framework.

We integrated all three models into the fault simulator [8] and the ATPG [15] and applied these tools to ISCAS benchmarks. Of particular interest was the validity of test vectors generated for the old Shockley model for newer models. This is related to the question whether new test generation is required after design shrinking.

The remainder of the paper is organized as follows: the general framework is described in the next section. Technology-specific I-V models are discussed in Section 3. Experimental results are reported in Section 4. Section 5 concludes the paper.

2 General Framework

Figure 1 (left) shows two nodes n_1 and n_0 bridged by a resistive short defect with resistance R_{sh}. We assume that gate D_1 drives the logic-1 value on n_1 and gate D_0 drives logic-0 on n_0, respectively. n_1 is connected to the inputs of gates A_1, A_2 and A_3 with logic gate thresholds Th_{A1}, Th_{A2} and Th_{A3}, respectively; n_0 drives gates B_1 and B_2 with the respective thresholds Th_{B1} and Th_{B2}. Figure 1 (right) shows possible voltage characteristics of the voltage V_{n1} on n_1 and V_{n0} on n_0 as a function of the bridge resistance R_{sh}. For

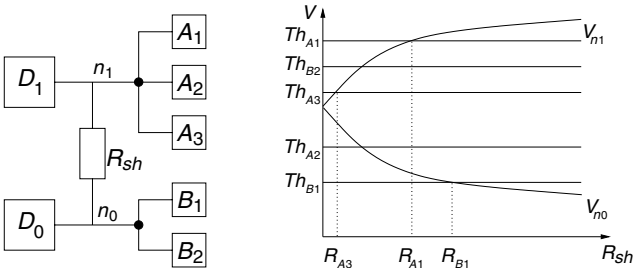

Figure 1: Example circuit and its R_{sh}-V diagram

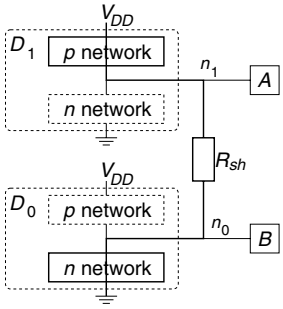

Figure 2: High-level electrical structure of example circuit

$R_{sh} = 0$ (non-resistive bridge), V_{n1} and V_{n0} assume the same intermediate value (note that this value corresponds to the voltage considered by Voting [19] and Biased Voting [20] models). With increasing bridge resistance, the voltages on n_1 and n_0 diverge; for an infinite R_{sh}, V_{n1} would equal V_{DD} and V_{n0} would equal 0V, which are the fault-free values.

Logic gate thresholds Th_{A1} through Th_{B2} are independent from bridge resistance. One possible distribution of gate thresholds is depicted in Figure 1 (right) as horizontal lines. Critical resistances are determined from the intersections of these lines with the R_{sh}-V characteristics. For instance, R_{A1} is the critical resistance for gate A_1, i.e. if the bridge resistance is below R_{A1}, then gate A_1 will interpret the (faulty) logic value of 0, while for $R_{sh} > R_{A1}$ it will interpret the fault-free value. Note that there is no critical resistance for Th_{A2}, as the horizontal line has no intersection with the voltage characteristic V_{n1}. This means that gate A_2 will interpret the (fault-free) logic-1 value irrespective of the bridge resistance and no faulty effect will be propagated through gate A_2 for this test vector. Similarly, there is a critical resistance for gate B_1 but none for gate B_2. We are interested in determining the critical resistance from the gate threshold analytically.

Figure 2 shows some electrical details of the example circuit. (For simplicity, only one gate is driven by n_1 and n_0, respectively.) Gates D_1 and D_0 internally consist of a p transistor network and an n transistor network. Since D_1 drives a logic-1 on n_1, its p network establishes a connection to V_{DD} while its n network is disabled. Similarly, the n network of gate D_0 establishes a connection to ground. We can ignore the n network of gate D_1 and the p network of gate D_0 for further analysis, as these networks are switched off. Due to the resistive short defect, there is a conducting path

[1] We used BSIM4.4.0 released in March 2004. It is available from the URL http://www-device.eecs.berkeley.edu/∼bsim3/bsim4.html.

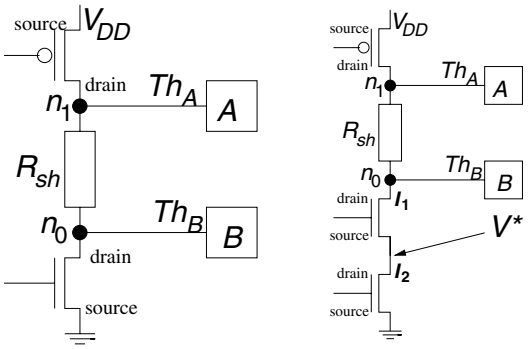

Figure 3: Low-level view of the two-inverter case and the inverter-NAND2 case

from V_{DD} to ground through the p network of gate D_1, the defect and the n network of gate D_0 (shown as the bold line in the figure). We call the current that is flowing through this path I_0, the voltage potentials on n_1 and n_0 are called V_{n1} and V_{n0}, respectively. Obviously, I_0, V_{n1} and V_{n0} are dependent on R_{sh}. Furthermore, the current flowing through n_1 and n_0 must be identical as there are no current sinks or sources on the path.

Suppose that the I-V_{ds} characteristics of the p transistor network of gate D_1 and the n transistor network of gate D_0 are given as $I_p(V_{ds})$ and $I_n(V_{ds})$, respectively. Then, the following system of equations must hold [5, 6]:

$$\left\{ \begin{array}{rcl} I_0 & = & I_p(V_{DD} - V_{n1}) \\ I_0 & = & I_n(V_{n0}) \\ R_{sh} & = & (V_{n1} - V_{n0})/I_0 \end{array} \right. \quad (1)$$

If the inverse functions of I_p and I_n are known, the calculation of the critical resistance for a given logic gate threshold is straightforward: let the threshold of gate A be Th_A. We are looking for the critical resistance R_A, i.e. for an R_{sh} value for which $V_{n1} = Th_A$. We calculate I_0 as $I_p(V_{DD} - V_{n1})$; then, we determine V_{n0} from I_0 using the inverse function I_n^{-1} and finally R_{sh} as $(V_{n1} - V_{n0})/I_0$. For computing the critical resistance for gate B, I_n and I_p^{-1} are used.

The proposed approach effectively reduces critical resistance calculation to computing I-V_{ds} characteristics of the transistor network under consideration. In the next section, we will demonstrate how to determine that I-V_{ds} characteristics for different transistor models. The general framework combined with an I-V_{ds} model yields a complete procedure for computing the critical resistance, which is required for simulating resistive bridging faults.

3 Technology-Specific Models

This section describes calculation of I-V_{ds} characteristics for p and n transistor networks. We present three different models: Shockley model, Fitted model and Predictive model. The Shockley model is based on conventional transistor equations that ignore some of the electrical phenomena in deep submicron technologies. The Fitted model uses equations with free variables that are fitted in order to match actual SPICE data. Finally, the Predictive model is again fully analytical and employs BSIM4 equations. Note that if a different I-V_{ds} model is in use (e.g. a company-internal solution), it can be integrated into the general framework in a straightforward way.

In the following, we describe the three models. We concentrate on the n transistor network, as the handling of the p network is largely identical. We start with the simple case in which the outputs of two inverters are bridged. In this case, both the p and the n network consist of just one MOSFET, respectively. This analysis is also valid for a network of parallel transistors (e.g. the p network of a NAND gate and the n network of a NOR gate). In this case, the equations for the inverter case must be updated by simply replacing $W_{NOT,n}$ by $k \cdot W_{NOR,n}$, where $W_{NOT,n}$ is the width of the n transistor in the inverter, $W_{NOR,n}$ is the width of each of the n transistors in the NOR gate, and k is the number of active n transistors under the given test vector. For serial connections of transistors (e.g. the p network of a NOR gate and the n network of a NAND gate), no such simple mapping exists. Figure 3 shows the two activated transistors in the two-inverter case (left) and the serial n network in a NAND2 gate bridged with an inverter (right).

3.1 Shockley Model

Shockley's conventional I-V_{ds} equation is given as

$$I_{ds,n}(V_{ds,n}) = \mu_n C_{ox} \frac{W_n}{L_n} \left((V_{gs,n} - V_{tn0}) V_{ds,n} - \frac{V_{ds,n}^2}{2} \right) \quad (2)$$

where μ_n is the mobility, C_{ox} the oxide capacity per area unit, W_n the channel width, L_n the channel length and V_{tn0} the zero bias threshold voltage for an NFET. Since the transistor is on, the gate voltage must be V_{DD} (logic-1). As the source terminal of the n transistor is connected to ground, the gate-source voltage $V_{gs,n}$ equals V_{DD} (see the left part of Figure 3).

The inverse equation I^{-1} (which yields voltage $V_{ds,n}$ for a given current I_0) is obtained by solving the quadratic equation $I_0 = I_{ds,n}(V_{ds,n})$. As described in the previous section, the critical resistance can be calculated using the I-V_{ds} equation and its inverse. Closed-form formulae for critical resistance in the Shockley model can be found in [5, 6, 8]. The equation for the critical resistance of a gate that succeeds the bridged line driven by the n network is given as

$$R_{crit,n} = \frac{|V_{tp0}| - Th + \sqrt{(V_{DD} - |V_{tp0}|)^2 - \frac{2 I_{ds,n}(Th)}{C_{ox} \mu_p W_p / L_p}}}{I_{ds,n}(Th)} \quad (3)$$

where Th is the logic threshold of the gate, V_{tp0}, μ_p, w_p and L_p are the zero bias threshold voltage, the mobility, the channel width and the channel length for a PFET, respectively, and $I_{ds,n}(Th)$ is calculated using Eq. (2). This equation is valid for a single transistor and a parallel transistor network (using an appropriate value for the width). For a serial network, *equivalent transistor calculation* is performed, which accounts for the body-bias effect. See [5] for details.

3.2 Fitted Model

The Fitted model uses the following I-V_{ds} equation for the n transistor network:

$$I_{ds,n}(V_{ds,n}) = A_n W_n \left((V_{DD} - B_n) V_{ds,n} - \frac{V_{ds,n}^2}{2} \right) \quad (4)$$

where A_n and B_n are obtained by fitting SPICE results. There are several sets of (A_n, B_n) parameters for different transistor configurations, which eliminates the need for the equivalent transistor calculation required in the Shockley model. Note that for $A_n = \mu_n C_{ox}/L_n$ and $B_n = V_{tn0}$, the Fitted model is identical to the Shockley model. We also performed experiments with the Alpha-Power Law model [21], which also involves fitting, but we obtained better results using Eq. (4). The R_{crit} equation for a gate with logic threshold Th driven by the n network is

$$R_{crit,n} = \frac{|B_p| - Th + \sqrt{(V_{DD} - |B_p|)^2 - \frac{2 I_{ds,n}(Th)}{A_p W_p}}}{I_{ds,n}(Th)} \quad (5)$$

where $I_{ds,n}(Th)$ is calculated using Eq. (4).

Table 1 shows critical resistance values calculated by HSPICE, the Shockley model and the Fitted model for different channel widths W_p and W_n (more results are available but omitted due to limited space). We consider the bridge between the outputs of two inverters and the bridge between two NAND gates (in the latter case we distinguish between one and two active p transistors): Note that the critical resistance values are for the gate A driven by the p transistor network for the two-inverter-bridge and for the gate B driven by the n transistor network for the two-NAND-bridge. It is clearly seen that the values computed by the Fitted model track the HSPICE values much better than the values obtained by the Shockley model. Even for the simple two-inverter case, the deviation of the Shockley model from the HSPICE reference is up to 5%; for the two-NAND case it sometimes exceeds 35%. In contrast, the Fitted model never has a deviation larger than 0.4%.

3.3 Predictive Model

3.3.1 Single transistor or parallel network

According to BPTM/BSIM4, the I-V_{ds} characteristic in the relevant V_{ds} region is described by the equation

$$I_{ds,n}(V_{ds,n}) = \frac{\frac{W_n}{L_n} \mu_{eff,n} Q_{ch0,n} V_{ds,n} \left(1 - \frac{V_{ds,n}}{2V_{b,n}}\right)}{1 + \frac{V_{ds,n}}{E_{sat,n} \cdot L_n}} \quad (6)$$

where $\mu_{eff,n}$ is the effective mobility, $Q_{ch0,n}$ is the channel charge density and $E_{sat,n}$ is the critical electrical field at which the carrier velocity becomes saturated. $V_{b,n}$ is defined as $(V_{gsteff,n} + 2v_t)/A_{bulk,n}$, where $V_{gsteff,n}$ is the effective $V_{gs,n} - V_{th,n}$, v_t is the thermal voltage ($k_B T/q$) and A_{bulk} models the bulk charge effect. All these parameters can be calculated from over 100 process parameter values. (Example values for 65nm and 45nm are given on the BPTM homepage [18]). In two-inverter case, V_{bs} is set to 0 and V_{gs} is set to V_{DD} for NMOS and $-V_{DD}$ for PMOS (see the left part of Figure 3). For parallel networks, the width W_n has to be set appropriately, as mentioned above.

	2-inverter bridge			2-NAND bridge, 1 active PFET			2-NAND bridge, 2 active PFETs		
W_p, μm	2	4	8	2	4	8	2	4	8
W_n, μm	1	2	4	1	2	4	1	2	4
	$R_{crit,A}$, Ω			$R_{crit,B}$, Ω			$R_{crit,B}$, Ω		
HSPICE	2422	1159	567	1686	838	418	4250	2064	1018
Shockley	2304	1152	576	2305	1152	576	4660	2330	1165
Fitted	2415	1157	566	1685	838	419	4266	2072	1019

Table 1: Results of Shockley and Fitted models compared to HSPICE; $L_p = L_n = 0.35\mu$m, $V_{DD} = 3.3$V, logic gate threshold = $V_{DD}/2$

Note that, as in the Shockley model and the Fitted model, the inverse function is obtained by solving a quadratic equation. In this way, BPTM/BSIM4 is relatively easy to integrate into the general critical resistance calculation framework. However, some of the parameters in Eq. (6) exhibit a second-order dependency on $V_{ds,n}$. This is because the transistor threshold depends on $V_{ds,n}$ through its DIBL (Drain-Induced Barrier Lowering) and DITS (Drain-Induced Threshold Shift) terms. The transistor threshold is required for the calculation of $V_{gsteff,n}$ and consequently into $Q_{ch0,n}$, $\mu_{eff,n}$ and $V_{b,n}$. When calculating $V_{ds,n} = I^{-1}(I_0)$, $V_{ds,n}$ is naturally unknown in advance. In order to account for this dependency, we applied the following iterative method: we calculated the parameters of Eq. (6) for $V_{ds,n} = 0$ and computed $V_{ds} = I^{-1}(I_0)$. Then, we re-calculated the parameters using that V_{ds} value and re-computed $V_{ds,n} = I^{-1}(I_0)$ using new parameters. We found that the maximal deviation from the old $V_{ds,n}$ value was maximally 2mV, and that changes in current were under 10^{-14} μA. Hence, this iteration can be omitted when optimizing for speed.

3.3.2 Serial network

Figure 3 shows the serial n transistor network of a NAND2 gate. We will first describe the calculation of I^{-1} (obtaining the voltage V_{n0} from the current I_0), and then the calculation of the current from the voltage.

We call the voltage between the two NFETs V^*. We can determine it as $I^{-1}(I_0)$ using essentially the same function that we used in the two-inverter case. To compute V_{n0} from V^*, we first set V_{bs} to $-V^*$ and V_{gs} to $V_{DD} - V^*$ and re-extract the parameters. Then, we apply I^{-1} once again and obtain some V'. Note that $V' < V^*$. Finally, V_{n0} is given as $V^* + V'$.

In order to calculate I_0 from V_{n0}, we use an iterative algorithm. We denote the current flowing through the lower NFET (connected to ground) as I_1 and the current flowing through the upper NFET as I_2. Obviously, I_1 and I_2 must be equal. Our algorithm modifies I_1 and I_2 until they become nearly the same. The algorithm uses the voltage V^* as the iteration variable.

(1) $V^* := V_{n0}/2$;
(2) Calculate I_1 (using I_{ds} formula for one transistor with $V_{ds,n} = V^*$, $V_{bs,n} = 0$, $V_{gs,n} = V_{DD}$)
(3) Calculate I_2 (using $V_{ds,n} = V_{n0} - V^*$, $V_{bs,n} = -V^*$, $V_{gs,n} = V_{DD} - V^*$)
(4) $I^* := (I_1 + I_2)/2$;
(5) **if** $(|I_1 - I_2| < \varepsilon)$ **return** I^*;
(6) Calculate V^* from I^* (using $V_{bs,n} = 0$, $V_{gs,n} = V_{DD}$)
(7) **goto** (2);

Note that the algorithm converges because $V_{n0} - V^*$ always holds after the first iteration. For ε = 1 μA, the algorithm always terminated after 6 iterations.

4 Experimental Results

We integrated the support of the Fitted and the Predictive models into the fault simulator [8] and the automatic test pattern generator [15], which already supported the Shockley model. We used HSPICE with a BSIM3v3 0.35 μm model card to obtain the values A_p, A_n, B_p and B_n for the Fitted model. For the Predictive model we used the 65nm BSIM4 model card available at the BPTM URL [18]. We applied ATPG and fault simulation to ISCAS 85 and combinational parts of ISCAS 89 (indicated as 'cs') circuits. The fault set consisted of 10,000 randomly selected non-feedback resistive bridging faults (where available). All measurements were performed on a 2GHz Linux machine with 1 GB RAM.

ATPG results are reported in Table 2. The table contains the name of the circuit, the number of considered faults, and the number of test vectors generated for the three technology-specific models. It can be seen that the number of generated test vectors varies across the models with no clear trend; it can not be claimed that the Fitted or the Predictive model are "more complex" from the ATPG's point of view, despite the non-trivial circuit behavior that they account for.

Note that, although the number of RBF test vectors is typically higher than the number of stuck-at test vectors generated by state-of-the-art ATPG systems [22, 23], the number of considered faults is also larger. It is demonstrated in [15] that the fault efficiency (i.e. the average number of faults detected by one test pattern) is higher for our tool than for other RBF ATPGs [4, 3] as well as stuck-at ATPGs.

We used our fault simulator to study the implications of *design shrinking*, i.e. manufacturing an existing device in a next-generation technology without actual redesign, for resistive bridging fault detection. We were interested in information whether the vectors generated for the old device are still valid for the new one. For this purpose, we generated the test vectors obtained by the ATPG under the Shockley model and performed fault simulation under the Fitted and the Predictive model. For calculating fault coverage, we employed the density function ρ of the short resistance derived from one used in [10] (based on data from [24]). Note that the number of applied vectors can be found in Column 3 of Table 2 and that their fault coverage under the Shockley model is always 100%.

Results can be found in Table 3. The vectors turn out to be very effective under the Fitted model (the coverage is 99.93% for circuit cs00832, 99.96% for circuit cs00820, 99.97% for circuit cs09234, and higher for all other circuits). The validity of the test vectors under the Predictive model is less distinctive. However, given the huge differences between the behavior of the transistors that Shockley's equations are supposed to model and the BPTM/BSIM4 ultra deep submicron model for 65nm, the fault coverages over 99% for 22 circuits out of 36 and over 97% for all but one circuit appear to be acceptable. Nevertheless, the results indicate at least a need for a new fault simulation run after a major design shrinking.

Circuit	#faults	Shockley	Fitted	Predictive
c0095	77	18	20	16
c0432	5253	732	659	489
c0880	10000	745	816	341
c1355	10000	178	240	243
c1908	10000	267	329	391
c2670	10000	366	371	459
c3540	10000	489	464	576
c5315	10000	384	382	419
c7552	10000	357	377	388
cs00208	3986	124	120	145
cs00298	4468	125	158	141
cs00349	7881	197	172	149
cs00382	7809	255	253	198
cs00386	9384	77	72	164
cs00400	8290	245	276	205
cs00420	10000	317	305	405
cs00444	10000	312	320	238
cs00510	10000	320	334	263
cs00526	10000	372	432	264
cs00641	10000	304	333	352
cs00713	10000	332	364	324
cs00820	10000	454	481	341
cs00832	10000	445	489	350
cs00838	10000	473	511	653
cs00953	10000	422	429	344
cs01238	10000	508	524	583
cs01423	10000	514	536	418
cs01488	10000	234	230	254
cs01494	10000	225	221	247
cs05378	10000	824	846	650
cs09234	10000	904	904	736
cs1196	10000	427	429	447
cs13207	10000	1228	1192	879
cs15850	10000	1060	1027	757
cs344	10000	143	138	134
cs35932	10000	516	726	607
cs38417	10000	1178	1114	732
cs38584	10000	1822	1883	1197

Table 2: ATPG results for the three models

Circuit	Fitted	Pred.	Circuit	Fitted	Pred.
c0095	99.98	99.76	cs00526	99.99	99.84
c0432	100.00	99.93	cs00641	100.00	98.86
c0880	100.00	99.92	cs00713	100.00	98.77
c1355	99.99	97.21	cs00820	99.96	99.49
c1908	99.98	99.24	cs00832	99.93	99.32
c2670	99.99	99.25	cs00838	100.00	97.43
c3540	99.99	98.62	cs00953	100.00	99.87
c5315	100.00	99.77	cs01238	99.98	97.69
c7552	99.99	99.85	cs01423	100.00	99.88
cs00208	100.00	97.48	cs01488	100.00	98.29
cs00298	99.98	99.69	cs01494	100.00	98.04
cs00349	100.00	97.96	cs05378	100.00	99.82
cs00382	100.00	99.91	cs09234	99.97	98.73
cs00386	100.00	91.88	cs13207	99.98	99.33
cs00400	100.00	99.91	cs15850	99.99	99.44
cs00420	100.00	97.36	cs35932	99.98	99.02
cs00444	99.99	99.88	cs38417	99.99	99.77
cs00510	100.00	99.83	cs38584	99.89	98.56

Table 3: Fault coverage of Shockley-ATPG vectors for Fitted and Predictive models

5 Conclusions

We presented three electrical-level models for calculating the critical resistance, which is required for accurate handling of resistive bridging faults. The models have a common general framework and technology-specific parts based on I-V_{ds} characteristics. We proposed a model for conventional technology described by Shockley equations, one valid for current submicron designs based on fitting SPICE data, and one intended for future nanoscale CMOS employing predictive transistor modeling with BSIM4. We integrated the support for all three models into our simulator and ATPG tools. It turned out that the test complexity, expressed in the number of vectors required for 100% fault coverage, does not show a trend towards one of the models. Moreover, we investigated the efficiency of test vectors generated for the Shockley model in detecting defects in submicron technologies using the two other models, in order to estimate the need for a new ATPG run after a design shrinking. Very high coverages are still obtained for all circuits under the Fitted model, but only for some circuits using the Predictive model, suggesting that a re-evaluation of fault coverage is required at least.

The models accurately reflect non-trivial electrical behavior in nanoscale technologies. However they concentrate on the static phenomena. Our further research will concentrate on modeling dynamic effects of the resistive short and open defects.

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